



Audio Engineering Society Convention Paper

Presented at the 114th Convention
2003 March 22–25 Amsterdam, The Netherlands

This convention paper has been reproduced from the author's advance manuscript, without editing, corrections, or consideration by the Review Board. The AES takes no responsibility for the contents. Additional papers may be obtained by sending request and remittance to Audio Engineering Society, 60 East 42nd Street, New York, New York 10165-2520, USA; also see www.aes.org. All rights reserved. Reproduction of this paper, or any portion thereof, is not permitted without direct permission from the Journal of the Audio Engineering Society.

They Exist: Limit Cycles in High Order Sigma Delta Modulators

J. D. Reiss and M. B. Sandler

Department of Electronic Engineering, Queen Mary, University of London,
Mile End Road, London E1 4NS, U.K.

ABSTRACT

A compact form can be used to describe an arbitrary high order sigma delta modulator. This provides insight into the structure of limit cycles in sigma delta modulators. We consider modulators of any order with periodic output. We make no assumptions regarding the input and are thus able to prove necessary conditions for limit cycles in the output. We show that the input must be periodic, but may have a different period from both integrator output and quantised output. We derive what this implies regarding limit cycles for sinusoidal inputs. Finally, we give examples where sinusoidal input to a third order modulator results in a limit cycle of a different frequency.

1. INTRODUCTION

Sigma delta modulators (SDMs) operate using a trade-off between oversampling and low-resolution quantization. A signal is sampled at much higher than the Nyquist frequency, typically with one bit quantization, so the signal may be effectively quantized with a high resolution. Recent work has concentrated on tone suppression[1], multibit modulation[2], compression[3, 4] and chaotic modulation[5]. Sigma delta modulators are used in A/D and D/A converters and in audio processing systems. The Sigma-Delta bitstream format is used for mastering and archiving of audio recordings[6, 7].

Unfortunately, sigma delta modulators are susceptible to limit cycle oscillations that are not present in the input signal. These idle tones may be audible to the listener when SDMs are used for audio signal processing. Considerable work has been done on the identification of

limit cycles in first and second order SDMs with constant input, but a general theory has not yet been formalized. Most previous analysis assumed constant input. This is invalid in most cases. Although the data is oversampled at a high rate, this is not sufficiently high as to make the input appear constant over a long sequence of samples. For situations where the limit cycle may be audible, i.e., high periodicity, the assumption of constant input has been violated. We extend existing theory and determine necessary conditions for the existence of limit cycles in SDMs with nonconstant input. We assume periodic behaviour in the output to determine input structures that lead to limit cycles. We derive theorems that classify the limit cycle behavior for different types of input, and the requirements to produce a limit cycle. These theorems are a contribution towards a general theory of limit cycles behaviour in SDMs of any order.

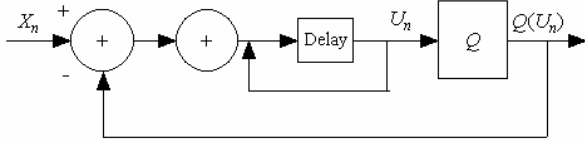


Figure 1. The simplest sigma delta modulator.

2. BACKGROUND

The simplest first order SDM, as depicted in Figure 1, consists of a 1bit quantizer embedded in a negative feedback loop which contains a discrete-time integrator. The input is sampled at a frequency higher than the Nyquist frequency and is converted into a binary output. The system may be represented by the map[8]

$$U_n = U_{n-1} + X_n - Q_{n-1} \quad (1)$$

where X represents the input signal, bounded by -1 and +1 and Q is the quantizer

$$Q_n = \begin{cases} 1 & \text{if } U_n \geq 0 \\ -1 & \text{if } U_n < 0 \end{cases} \quad (2)$$

All of the following calculations are valid for a different or multilevel quantizer, with suitable scaling. In this representation, the output Q_n represents the quantization of input X_{n-1} . On average, the quantized output will be approximately equal to the input. This system works by quantizing the difference between the input and the accumulated error. When the error grows sufficiently large, the quantizer will flip in order to reduce the error.

A typical commercial implementation of a sigma delta modulator is far more complicated. It uses multiple loops to assist in the shaping of the noise. Gain terms are used to enforce stability[9], to refine noise shaping, or due to integrator leakage[10]. Quantized output is not determined solely by the previous input and the accumulated error. Initial conditions can not always be set to 0. These higher order modulators are often less stable and analysis becomes problematic.

3. COMPACT REPRESENTATION

We begin with a simple form of high order modulator, represented in Figure 2. We note first that some sigma delta modulators may not fit this form[11], since gain terms are sometimes placed after the delay term. However, many practical implementations of SDMs fit the form of Figure 2, and this representation includes the generic models of first and second order sigma delta modulators with integrator leak such as in [12].

Gain terms are represented by p_1, p_2, \dots, p_N . They may be imposed in order to give the SDM specific noise shaping characteristics, or due to circuit imperfections. If all gain terms are unity, this reduces to the generic first or second order stable modulators that have been studied extensively throughout the literature. $B_{m,n}$ represents the

input to the m^{th} accumulator due to the n^{th} input to the sigma delta modulator. Due to the action of an accumulator in Figure 2, the following recursive relationship holds for the m^{th} accumulator,

$$B_{m+1,n} = (B_{m,n} - B_{m,n-1})q_{m+1} + Q_n \quad (3)$$

Where for any n and m , $B_{0,n} = U_{n+1}$, $B_{N,n} = X_n$ and $q_m = 1/p_m$.

By induction, (3) leads to the following compact form for an N^{th} order SDM.

$$X_n = \sum_{j=0}^N (-1)^j \binom{N}{j} U_{n-j+1} \prod_{k=1}^N q_k + \sum_{i=0}^{N-1} \sum_{j=0}^i (-1)^j \binom{i}{j} Q_{n-j} \prod_{k=1-i}^0 q_{N+k} \quad (4)$$

Or equivalently, for any N^{th} order modulator at time n ,

$$U_{n+1} = X_n \prod_{k=1}^N p_k - \sum_{j=1}^N (-1)^j \binom{N}{j} U_{n-j+1} - \sum_{i=0}^{N-1} \sum_{j=0}^i (-1)^j \binom{i}{j} Q_{n-j} \prod_{k=1}^{N-j} p_k \quad (5)$$

A full derivation of these formulas is given in [13]. Equation (5) provides a compact representation which represents current integrator output (and hence current quantized output) as an explicit function of the last input and the N previous integrator outputs.

This simplifies the math used in analysis of sigma delta modulators, and because it allows for fast simulation (and realization) of such a system. Similar compact representations can be devised for positioning the gain terms elsewhere in the noise shaping loop, or for other modulator designs. However, these forms do not always yield a simple analysis of limit cycle behavior.

4. LIMIT CYCLE BEHAVIOR

Assume that the integrator output, U is periodic with period P_U , so

$$(\forall n)[U_{n+P_U} = U_n] \& (\forall r < P_U)(\exists n)[U_{n+r} \neq U_n] \quad (6)$$

The second half of (6) was included to indicate that the period is not a divisor of U_p . The first consequence of this is that Q must be periodic, since the quantizer Q_n is strictly a function of U_n . If we sum the input signal over one period and interchange summations, then (4) leads to

$$\sum_{r=1}^{P_U} X_{n+r} = \sum_{j=0}^N (-1)^j \binom{N}{j} \sum_{r=1}^{P_U} U_{n+r-j+1} \prod_{k=1}^N q_k + \sum_{i=0}^{N-1} \sum_{j=0}^i (-1)^j \binom{i}{j} \sum_{r=1}^{P_U} Q_{n+r-j} \prod_{k=1-i}^0 q_{N+k} \quad (7)$$

Using the periodicity of Q and U , and interchanging summations, it can be shown[13] that this reduces to

$$\sum_{r=1}^{P_U} X_{n+r} = \sum_{r=1}^{P_U} Q_{n+r} \quad (8)$$

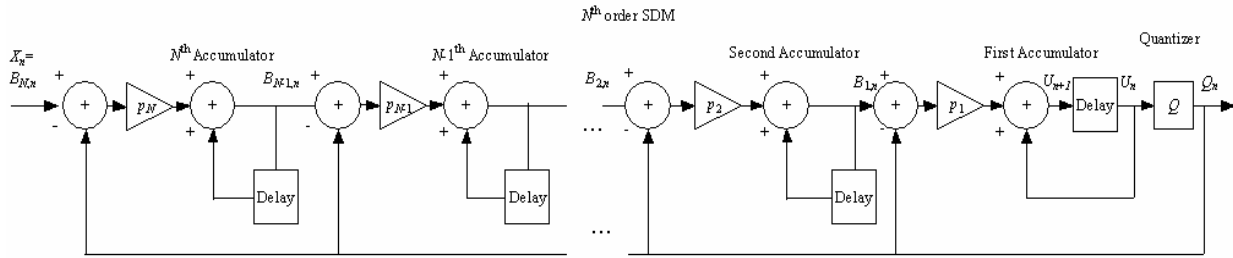


Figure 2. Block diagram of a high order sigma delta modulator.

This shows that the quantized output over one period depends only on the input over one period, and not directly on the integrator outputs U or the gain terms p . If the period of X is 1, then this becomes constant input and the conclusions of previous authors are valid[10-12]. Also, since U is periodic and Q_n depends solely on U_n , the period of Q , P_Q , must be a divisor of P_U , and is possibly equal to P_U . From (8),

$$X_{n+P_U} - X_n = \sum_{r=1}^{P_U} X_{n+r} - X_{n+r} = \sum_{r=1}^{P_U} Q_{n+r} - Q_{n+r-1} = 0 \quad (9)$$

So the period of X , P_X is a divisor of P_U , although it is not necessarily equal to the period of Q . Using these relationships, it can be proven that P_X is the smallest positive integer such that for all n , $\frac{P_U}{P_X} \sum_{i=1}^{P_X} X_{i+n} = \sum_{i=1}^{P_U} Q_{i+n}$. This is demonstrated in all simulations depicted in Table 1. So for a two level quantizer of the form given in (2), $\sum_{i=1}^{P_U} X_{n+i} = c$ where c is an integer such that $-P_U \leq c \leq P_U$.

Equation (7) has further implications. It is possible for $P_X \neq P_U \neq P_Q$, as shown in Table 1. P_U is the fundamental period, in the sense that both P_X and P_Q must be divisors of P_U . The quantized output can have a shorter period than that of the sampled input. Limit cycles appear in the power spectrum as sharp peaks. Hence this is problematic because it implies a significant difference between the frequency of the input and output signals. This can result in phantom frequencies in the output of sigma delta modulation when used in audio processing. This effect may be avoided by using alternative modulator designs. It may be minimised through the addition of dither, which breaks up limit cycles.

5. SINUSOIDAL INPUTS

Consider sinusoidal input, $A \sin(2\pi f_0 t + \mathbf{f})$. This does not guarantee periodic output. Initial conditions, quantization levels, gain terms, and sampling

frequency all have an effect on whether periodic output is produced. Suppose the sampling frequency f_s , and the sine wave frequency f_0 , have a common denominator, $f_s = f_0 a/b$. Then the input is periodic with period a and the necessary condition for periodic output is satisfied. In an SDM with real world input, these assumptions may be approximately true or true for a limited input sequence.

Now assume that the sampling frequency is some integer multiple, greater than one, of the sine wave frequency, $f_s = f_0(c+1)$. Then it can be shown that over one period, the sum of the input over one period of the sine wave is 0, regardless of phase.

$$\sum_{r=1}^{c+1} A \sin(2\pi f_0(r/f_s) + \mathbf{f}) = 0 \quad (10)$$

Equation (8) implies

$$\sum_{r=1}^{c+1} Q_{n+r} = 0 \quad (11)$$

This is a simple requirement for limit cycles to exist with the same period as the sinusoidal input. It has no dependence on the phase or amplitude of the waveform, the initial conditions of the integrators and quantizers, or the gain terms in the modulator design. If the modulator design does not allow for (11) to hold, then we have a situation where a frequency exists in the input but not in the output.

$\sum_n X_n$	P_X	P_U	P_Q
3/5	3	15	5
2/3	2	6	3
3/2	3	6	2
3/2	3	6	6
1/2	3	6	6
1/3	2	6	6
1/3	3	9	9
2	3	3	3

Table 1. Simulations from a first order SDM without gain. Quantised values are either 0 or 1.

These arguments can be extended to find similar conditions for the existence of limit cycles with other types of input, such as the sum of several sinusoids, or sinusoids with a different relationship between sampling frequency and Nyquist frequency.

6. DEPENDENCE ON INITIAL CONDITIONS

In Section 4, we showed that (6) was necessary for limit cycle behavior in the integrator output. In the case of a first order modulator, this is also a sufficient condition. This can be shown by assuming that it holds for a first order SDM, e. g., for some P ,

$$\sum_{s=1}^P X_{n+s} = \sum_{s=1}^P Q_{n+s} \quad (12)$$

As can be seen from Figure 2 or Equation (5) with $N=1$, for a first order SDM with gain, the integrator output is given by

$$U_{n+1} = U_n + p_1 X_n - p_1 Q_n \quad (13)$$

So we can apply this formula P times to derive U_{n+P} as a function of U_n .

$$U_{n+P} = p_1 \sum_{i=0}^{P-1} X_{n+i} + U_n - p_1 \sum_{i=0}^{P-1} Q_{n+i} = U_n \quad (14)$$

and we can similarly show that if (12) does not hold for some value r smaller than P , then the integrator output can not have period r . That is,

$$(r < P) \Rightarrow (\exists n)[U_{n+r} \neq U_n] \quad (15)$$

So (8) is a necessary and sufficient condition for periodicity in a first order SDM. Periodicity is independent of initial conditions and gain terms. Furthermore, we can determine if periodic behavior is possible for an input by looking at the allowable quantiser states. Unfortunately, we cannot say the same about higher order modulators. Consider a second order modulator where we attempt to repeat Equations (12) to (14) for period 3. If we sum the difference equations and make use of (8),

$$U_{n+3} = U_n + (p_1 Q_{n-1} - p_1 Q_{n+2} + U_{n+2} - U_{n-1}) \quad (16)$$

Thus, in general, (8) is not a sufficient condition for periodic behaviour in second and higher order modulators. It is only a necessary one. On the other hand, if we assume period three behaviour then the difference equations yield,

$$3(U_{n+1} - U_n) = p_1 p_2 X_n - p_1 p_2 X_{n+1} - p_1(2 + p_2)Q_n + p_1 Q_{n+2} + p_1(1 + p_2)Q_{n+1} \quad (17)$$

So integrator output depends explicitly on input, quantised output values, gain and previous integrator output. Since U_2 is a function of U_0 and U_1 , (17) states that one can not set U_0 and U_1 arbitrarily and still have periodic behaviour beginning at U_2 . In other words, the initial conditions must be specified for a given period with given quantised output.

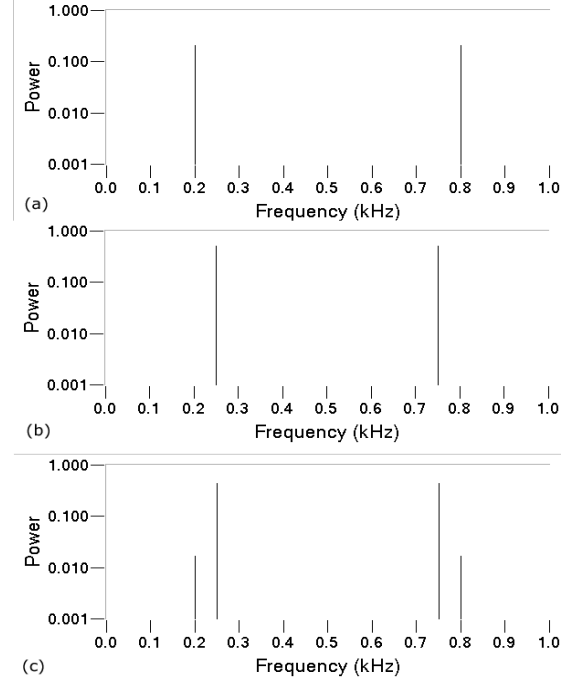


Figure 3. Power spectra for a third order SDM with $P_X=5$, $P_Q=4$, and $P_U=20$. (a) represents input, (b) quantized output and (c) integrator output. Ideally, these spectra would be identical with the exception of artifacts that could be easily filtered.

In general, an N^{th} order SDM requires N initial conditions, of which only 1 can be set arbitrarily for periodic output. This dependence on initial conditions is often neglected in the literature on limit cycles in sigma delta modulators, yet its implications are huge. Although, as shown, limit cycles may exist in high order modulators, and with nonconstant input, dependence on initial conditions guarantees that they are rare. Furthermore, with higher order modulators there are more initial conditions to set. Thus we have revealed an additional benefit of high order sigma delta modulation: the decreased likelihood of the existence of unwanted limit cycles.

7. RESULTS

The results in Table 1 were easy to find because they were from a first order SDM and had no dependence on initial conditions. In order to show the validity of this work, limit cycles must be found for nonconstant (possibly sinusoidal) input in high order modulators, and produce output periods different from the input period. A linear equation solver was used to find initial conditions that give limit cycles. Due to instability and sensitivity to small errors, periodic behavior is not guaranteed. Still, the conclusions have been verified in numerous simulations.

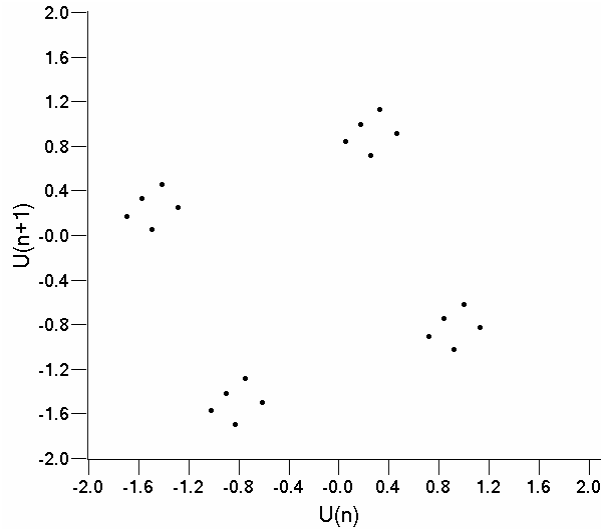


Figure 4. A delay coordinate embedding plot of the period 20 integrator output. 2^{14} samples have been plotted and it is clear that period 20 behavior persists throughout the entire data set.

Sinusoidal input, $0.97\sin(2\pi n/5+0.71\pi)$, was applied to a third order SDM such that the input had period 5. Gain terms were set to $p_1=0.91$, $p_2=0.66$ and $p_3=0.77$, $U_0=0.8$, and U_1 and U_2 were determined using a linear equation solver to find initial conditions that gave periodic behavior with $P_Q=4$, $P_U=20$. In practical situations these conditions could occur through appropriate input before periodic input commences.

This system produced the extreme situation of $P_x \neq P_U \neq P_Q$. As depicted in Figure 3, it resulted in different power spectra for input, integrator output, and quantiser output. Assuming the input signal was in the audible range, the differing frequencies that appear are of a high enough power that they would be audible and could not be simply filtered.

Although $P_U=20$, it does not result in a peak at 0.05 kHz. The limit cycle need not correspond with sinusoidal behavior. Peaks occur at 0.2 and 0.25 kHz. Figure 3(b) reveals that quantization erases evidence of the input frequency. This effect is also revealed in Figure 4, where successive values of U_n are plotted against each other. The 20 values are grouped into 4 groups of 5, where the 5 values in a group correspond to 5 input values, and the 4 groups correspond to possible quantization values Q_n and Q_{n+1} .

The structure and combinations of limit cycles that may exist are rich and diverse. Consider setting $p_1=0.27$, $p_2=0.65$ and $p_3=0.20$ with initial conditions $U_0=0.19$, $U_1=-0.109952$ and $U_2=0.191989$. A period 3 limit cycle input is applied, $X_n=0.17$, $X_{n+1}=0.31$ and $X_{n+2}=-0.48$ (such a limit cycle could also have been produced by sinusoidal input).

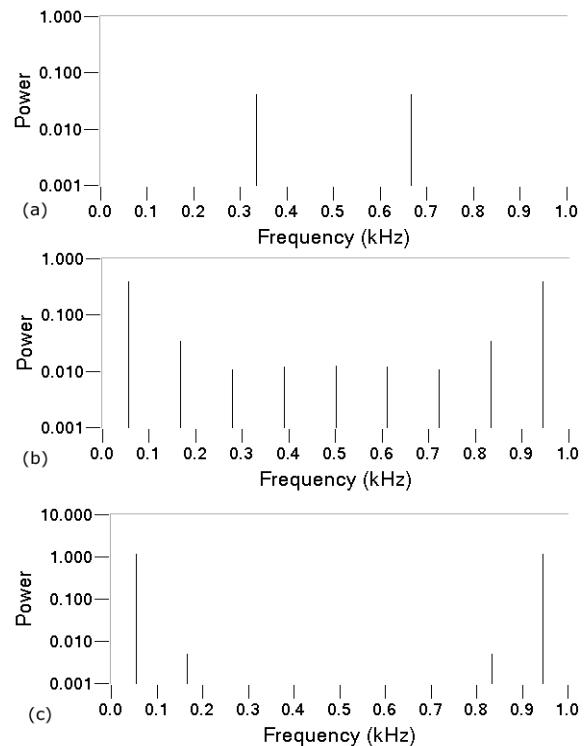


Figure 5. Power spectra for a third order sigma delta modulator where the input has period 3, and both quantized output and integrator output have period 18. (a) represents the power spectrum for the sinusoidal input, (b) for the quantized output and (c) for the integrator output before quantization. Despite the fact that quantized output and integrator output have the same period, they exhibit very different power spectra.

This results in both integrator output and quantized output having period 18. However, as indicated in Figure 5, they exhibit very different power spectra, neither of which bears much relation to the original input spectrum. An explanation is given by viewing the time delay plot of integrator output, Figure 6. Rather than the points being grouped into four regions as in Figure 4, the points follow a path around an ellipse, with symmetry broken only when the quantiser flips.

The quantized values consist of a sequence of 9 ones followed by 9 minus ones. Quantization destroys nearly all information regarding the output, and leaves only information concerning its period. This explains why Figure 5(b) shows no evidence of simple sinusoidal behavior. One may interpret this as indicating that information regarding the input signal is lost first through integration, and further destroyed by quantization. This is another indication that problematic limit cycles must be avoided.

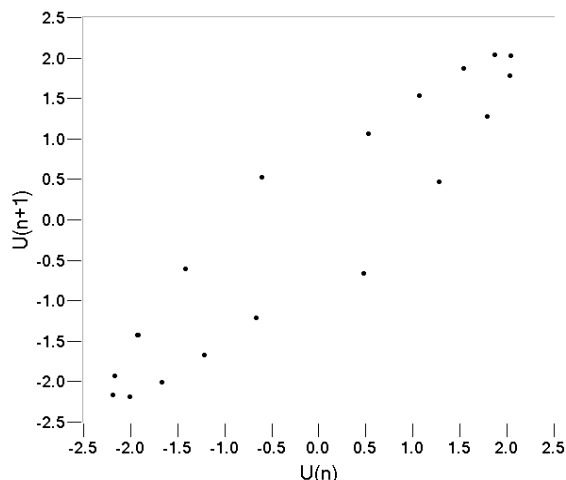


Figure 6. A delay coordinate embedding plot of the period 18 integrator output. Values follow a path around half an ellipse, until the quantizer flips, and the mirror image of the path is followed.

8. CONCLUSION

We showed that a compact form can be used to represent high order sigma delta modulators. This representation allows us to prove that periodic integrator output implies periodic input, and that the average output over one period depends on the average input. Because the two periods may differ, a limit cycle in the input signal may result in a limit cycle of different length occurring in the output.

For a first order modulator, equivalence of average input and average quantized output over a number of iterations is a necessary and sufficient condition that will guarantee periodic behavior. For second and higher order modulators, this is only a necessary condition. Initial conditions must also be found. Nevertheless, as verified by simulations in high order sigma delta modulators, these limit cycles do exist and can result in the input frequency being removed in the output, or replaced by different frequencies.

The theoretical results can be used to analyze the conditions for periodic output in the case of sinusoidal input. For instance, it was shown that a pure sine wave input with a Nyquist frequency that is a multiple of the sampling frequency can produce periodic output only if the sum of the quantizer output is zero over one period.

A framework has been laid down for further analysis. Ongoing work is being made to show both necessary and sufficient conditions for limit cycle behavior in a variety of sigma delta modulator designs. Cascaded or multistage modulator designs may be analyzed using similar techniques. An inverse approach, assuming limit cycles in the input, may be used with some designs to prove the existence of limit cycles in the

output. This is more difficult because of the effects of initial conditions on quantizer and integrator outputs.

9. ACKNOWLEDGMENT

The authors gratefully acknowledge Derk Reefman of Philips Research in Eindhoven and Orla Feely of University College Dublin for their insightful comments and criticisms concerning this work.

10. REFERENCES

1. Magrath, A. and M. Sandler, *Efficient Dithering of Sigma-Delta Modulators with Adaptive Bit Flipping*. Electronics Lett., 1995. **31**(11).
2. Park, S.J., R.M. Gray, and W. Chou, *Analysis of a sigma delta modulator with a multi-level quantizer and a single-bit feedback*, in *Proceedings of the ICASSP 91*. 1991: Toronto, Canada. p. 1957-1960.
3. Reiss, J.D., et al. *Improved Compression of DSD for Super Audio CD*. in *112th Convention of the AES*, 2002. Munich, Germany.
4. Reiss, J.D. and M.B. Sandler. *Efficient compression of oversampled 1-bit audio signals*. in *111th AES Convention*. 2001. NY, NY, USA.
5. Reiss, J. and M.B. Sandler, *The Benefits of Multibit Chaotic Sigma Delta Modulation*. CHAOS, 2001. **11**(2): p. 377-383.
6. Reefman, D. and E. Janssen. *Enhanced Sigma Delta Structures for SACD applications*. in *112th AES Convention*. 2002. Munich, Germany.
7. Reefman, D. and P. Nuijten. *Why Direct Stream Digital is the best choice as a digital audio format*. in *110th AES Convention*. 2001. Amsterdam, the Netherlands.
8. Gray, R.M., *Oversampled Sigma-Delta Modulation*. IEEE Transactions on Communications, 1987. **COM-35**: p. 481-487.
9. Farrell, R. and O. Feely, *Bounding the integrator outputs of second order sigma-delta modulators*. IEEE Trans. on Circ. and Syst., II, 1998. **45**.
10. Feely, O. and L.O. Chua, *The effect of integrator leak in S-D modulation*. IEEE Trans. on Circuits and Systems, 1991. **CAS-38**(11): p. 1293-1305.
11. Candy, J. and G. Temes, *Oversampling delta-sigma Data Converters*. 1991: IEEE Press.
12. Friedman, V., *The Structure of limit cycles in sigma delta modulation*. IEEE Trans. Communication, 1988. **36**(8): p. 972-979.
13. Reiss, J.D. and M.B. Sandler, *The Existence and Structure of Limit Cycles in High order Sigma Delta Modulators*. submitted to IEEE Transactions on Circuits and Systems - II, Analog and Digital Signal Processing, October 2002.