Audio Engineering Society

Convention Paper

Presented at the 117th Convention
2004 October 28–31 San Francisco, CA, USA

Description of Limit Cycles in Feedback Sigma Delta Modulators

Derk Reefman[1], Joshua D. Reiss[2], Erwin Janssen[1], and Mark Sandler[2]

[1] *Philips Research, 5656 AA Eindhoven, The Netherlands*

[2] *Queen Mary, University of London, E14 NS, United Kingdom*

Correspondence should be addressed to Josh Reiss (josh.reiss@elec.qmul.ac.uk)

ABSTRACT

The authors have recently developed a framework for analysis of limit cycle behavior in feedforward sigma delta modulators (SDMs). However, the dynamics of feedback SDMs appear to be completely different. Here, we extend that framework to include limit cycles in feedback SDMs. We prove that for DC inputs, periodic output implies state space periodicity. An outcome of this is that for an N^{th} order SDM, at least $N-1$ initial conditions must be fixed in order to have limit cycle behaviour. We present expressions for the minimum disturbance of the input or initial conditions that is needed to break up a limit cycle. These expressions are notably different from the analogous expressions for feedforward SDMs. We show that dithering the quantiser is a sub-optimal approach to removing limit cycles, and limit cycle stability is determined. Examples are provided that illustrate the theoretical results, and these results are also compared with those found for feedforward SDM designs. It is shown that, with respect to limit cycle behaviour, it makes little difference whether feedforward or feedback designs are used.

1. INTRODUCTION

One-bit Sigma Delta based analog-to-digital and digital-to-analog converters are widely used in audio applications, such as cellular phone technology and high-end stereo systems. In particular, it has seen a further boost in interest due to the introduction of Super Audio CD (SACD). SACD is based on a 1-bit coded representation of the audio stream with a sample rate of 2.8 MHz, and Sigma Delta modulation is clearly one of the techniques that is capable of creating a high-quality 1-bit stream.

Sigma Delta modulation is a well-established technique yet theoretical understanding of the concept is very limited [1]. The most important progress in the description of sigma delta modulators is reported in the theses of Risbo [8] and Hein [4], while a useful linearization technique is described in [10] and further elaborated in the thesis of Magrath [7]. Yet in all these developments, there is no unified description of SDMs.

Recent work by the authors [12, 13] has made significant progress towards developing a framework to describe the nature of limit cycles (LCs) in feedforward SDMs. Within this framework, several aspects of the feedforward SDM can be quantitatively understood. However, in various situations a feedback SDM is preferred over a feedforward one. Typically, this is due to the intrinsic anti-aliasing effect of the signal transfer function of a feedback SDM compared to a feedforward SDM [1].

In this paper, we will extend that framework to incorporate feedback SDMs. We will use as a definition of a limit cycle a sequence of P output bits, which repeats itself indefinitely. The basis for this approach has been provided in previous work, most notably in [4] and [9]. Along the lines presented in [13], we derive results for a general feedback SDM and focus on the character of the LCs, and their stability in particular. An important assumption in earlier work is that a periodic bit pattern implies periodicity in the state variables. This assumption was proven for feedforward designs, and will be proven for feedback designs in this paper. Based on a state space description, we present an exact description of limit cycles in feedback SDMs. While drawing on some known results from linear algebra, some remarkable results for limit cycles in SDMs are obtained, such as the persistance of limit cycles while dithering the SDM. Although in its pure definition, a limit cycle is a periodic pattern of infinite duration, in practical situations finite duration periodic sequences can be equally annoying. The finite duration patterns touch upon the important subject of stability of a limit cycle: how much time it takes until a small perturbation moves a limit cycle out of its periodic pattern.

The paper is organized as follows. In Sec. 2, the mathematical framework, based on a state space description of the SDM, is presented. All the following chapters are based on this formulation. In Sec. 3, this formulation is applied to practical SDM designs. Some basic quantitative criteria, necessary for determining the stability of a limit cycle, are developed. In Sec. 4, a stability analysis of limit cycles is presented. In Sec. 5, the concepts of the foregoing sections will be used to obtain numerical results, and

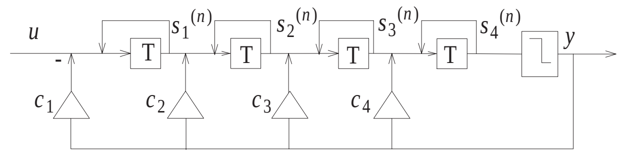

Fig. 1: *States in a 4th order SDM.*

these results will be contrasted with those found for feedforward SDM designs. Finally, in Sec. 6, conclusions will be presented.

2. MATHEMATICAL BACKGROUND

2.1. State Space description

Though state-space descriptions of discrete time processes are well-established [2], in this section we will review some of their aspects in order to present the paper in a self-contained way. In Fig. 1, the general topology for a distributed feedback SDM is depicted, in this case a fourth order SDM. This represents a typical feedback modulator design, which is often used in practical designs [11]. We can easily see that, for the modulator presented here,

$$\begin{aligned} s_N^{(n)} &= (0,..0,1)\mathbf{s}^{(n)} \\ y^{(n)} &= \mathrm{sgn}(s_N^{(n)}) \end{aligned} \tag{1}$$

where $y^{(n)}$ is the output bit at clock cycle n, and $s_i^{(n)}$ are the integrator outputs, called state variables. The last integrator output, $s_N^{(n)}$, is also the quantizer input signal.

The propagation of the states $\mathbf{s}$ can be written in matrix notation as:

$$\mathbf{s}^{(n+1)} = \mathbf{A}\mathbf{s}^{(n)} - y^{(n)}\mathbf{c} + u^{(n)}\mathbf{d} \tag{2}$$

where $\mathbf{c}$ is a vector of feedback coefficients, $\mathbf{A}$ is an $N \times N$ transition matrix for an SDM of order N, and $\mathbf{c} = (c_1, \ldots, c_N)^T$ and $\mathbf{d} = (1, 0, ...0)^T$ describe how the input and feedback, respectively, are distributed.

It is interesting to compare this with the equivalent feedforward design, where the state space equations are given by,

$$\begin{aligned} y^{(n)} &= \mathrm{sgn}(\mathbf{c}^T\mathbf{s}^{(n)}) \\ \mathrm{s}^{(n+1)} &= \mathbf{A}\mathbf{s}^{(n)} + (u^{(n)} - y^{(n)})\mathbf{d} \end{aligned} \tag{3}$$

For both designs, the placement of the transition matrix $\mathbf{A}$ in the state space equations is identical. However, for feedforward designs, the coefficient vector has no direct effect on the state space variables $\mathbf{s}$, and only acts as a weighting term on the quantisation. Whereas for the feedback design, the coefficient vector $\mathbf{c}$ acts as a constant that is added or subtracted from the state space variables every iteration. As we shall see, this implies that the dynamics of feedback and feedforward designs are very similar.

The power of the state space description is that it allows us to create a very compact description of the propagation of the SDM from time $t = 0$ to time $t = n$, as repeated application of Eq. (2) to $\mathbf{s}^{(0)}$ leads to $\mathbf{s}^{(n)}$:

$$\mathbf{s}^{(n)} = \mathbf{A}^n \mathbf{s}^{(0)} + \sum_{i=0}^{n-1} \mathbf{A}^{n-i-1}(u^{(i)}\mathbf{d} - y^{(i)}\mathbf{c}) \tag{4}$$

From the above equation, we can clearly see that the initial integrator states are simply a kind of an offset to the signal, even though they directly influence the output bit pattern. The spectrum of the signal is determined completely by the second term in the right-hand side of Eq. (4); the first term carries no signal information. Hence, this confirms the known fact that the signal content of a SDM modulator is not determined by its initial integrator states.

2.2. General formulation of limit cycle conditions

In the introduction, we have introduced the following definition of a limit cycle:

A limit cycle is a sequence of P output bits, which sequence repeats itself indefinitely.

The compact representation Eq. (4) gives the means to directly view the consequences of a limit cycle. In dynamical systems theory, a limit cycle of period P exists if, for initial conditions $s^{(0)}$,

$$\mathbf{s}^{(P+n)} = \mathbf{s}^{(n)} \tag{5}$$

for all n greater than or equal to zero. However, from a practical point of view, we are interested in periodic behavior in the output y. It is proven in App. 1 that, under reasonable assumptions, periodicity in y guarantees that a limit cycle exists. Thus we can use the limit cycle definitions, and as a consequence, we have a strict set of necessary (but not sufficient!) equalities that need to hold for the initial states if periodic output is to be sustained:

$$\begin{aligned}(\mathbf{I} - \mathbf{A}^P)\mathbf{s}^{(0)} &= \sum_{i=0}^{P-1} \mathbf{A}^{P-i-1}(u^{(i)}\mathbf{d} - y^{(i)}\mathbf{c}) \\ &\equiv \mathbf{L}_P(\{y^{(i)}\})\end{aligned} \tag{6}$$

where $\mathbf{L}_P(\{y^{(i)}\}$ has been introduced to avoid cumbersome notation. So we formally have

$$\mathbf{s}^{(0)} = (\mathbf{I} - \mathbf{A}^P)^{-1}\mathbf{L}_P(\{y^{(i)}\}) \tag{7}$$

From Eq. (6), we can obtain a *unique* value for the initial state $s^{(0)}$ if, and only if, the inverse of the matrix $(I - \mathbf{A}^P)$ exists. This will be elaborated in Sec. 3; for now, we assume that a solution or solution space to Eq. (7) exists.

So far, the appearance of the limit cycle has not been specified, except that it is of period P. It is an important observation, that a specific value for the initial state *only* determines the length of a limit cycle; it does not say anything yet about the sequence of 1s and -1s. However, if a limit cycle is now defined as a specific sequence $\{y^{(i)}\}(i = 1, \ldots, P-1)$, we have that for each $y^{(i)}$:

$$y^{(i)} s_N^{(i)} > 0 \tag{8}$$

which is a test that has to be passed if a limitcycle of the specified sequence $\{y^{(i)}\}(i = 1, \ldots, P-1)$ exists. The inaccuracy made in Eq. (8) is that the possibility that $v^{(i)}y^{(i)} = 0$ has been left out. As this equality occurs with probability zero over the continously variable value of $v^{(i)}y^{(i)}$, this should not pose much of a problem. We thus have a set of equalities, Eq. (6), and a set of inequalities, Eq. (8), that need to be fullfilled in order to have a valid limit cycle. If we substitute Eq. (4) in Eq. (8), we obtain:

$$\begin{aligned} &k = 0, ...P-1: \\ &y^{(k)}(0, ...0, 1)[\mathbf{A}^k \mathbf{s}^{(0)} + \mathbf{L}_k(\{y^{(i)}\})] > 0\end{aligned} \tag{9}$$

using the notation of Eq. (6).

Hence, we need to simultaneously solve Eq. (6) and Eq. (9) in order to have a valid limitcycle; in the next section more specific solutions will be derived for various SDM topologies.

3. LIMIT CYCLE CONDITIONS FOR SPECIFIC SDM ARCHITECTURES

In order to quantify the importance of any disturbance of a limit cycle, we first need to solve Eq.(7). However, in the previous section, the remark has been made that the matrix $(\mathbf{I} - \mathbf{A}^P)$ may not be invertible. This observation carries significant practical relevance. The poles of the loop filter of an SDM are given by the eigenvalues of the transition matrix $\mathbf{A}$: each pole p_i can be written as $p_i = \rho_i e^{j\omega_i}$, where ω_i is the pole frequency [4]. Hence, for a classical SDM which has all its loopfilter poles at DC, all eigenvalues of $\mathbf{A}$ will be one, as a result of which the inverse of Eq. (6) does not exist - hence, there is no unique solution to $\mathbf{s}^{(0)}$. Other SDM designs, such as those with resonator sections, may result in an invertible transition matrix. As a result, there would exist one - and one only - initial state $\mathbf{s}^{(0)}$ that results in a specific limit cycle. Most often, SDMs have at least a single zero at DC to avoid DC drift. In the following, we will make a separation in two main categories of SDMs: those with and without poles at DC. The SDMs with poles at DC will be further subdivided in two categories: those with poles at DC for the last two integrator sections; and those with poles away from DC for the last two integrator sections.

A special case of limit cycle break up is due to *dithering* the SDM. Typically, dithering is achieved by adding a random number to the input of the quantizer, which therefore adds a random element to the quantization process. Because it is a special, but important case, and as its effectiveness is strongly related to the limit cycle conditions, its discussion is included in Sec. 3.3.

3.1. SDMs with DC poles

In the case that the SDM has at least one of its poles at DC, the matrix $\mathbf{I} - \mathbf{A}^P$ is singular, and hence not invertible. To solve Eq. (6) for that case, we create the singular value decomposition (SVD)[3] of $(\mathbf{I} - \mathbf{A}^P)$:

$$(\mathbf{I} - \mathbf{A}^P) = \mathbf{U}\mathbf{\Sigma}\mathbf{V}^T \tag{10}$$

where $\mathbf{\Sigma} \in \mathbb{R}^{N\times N}$ is a diagonal matrix whose elements σ_i are the singular values of $\mathbf{I} - \mathbf{A}^P$. The matrices $\mathbf{U} \in \mathbb{R}^{N\times N}$ and $\mathbf{V} \in \mathbb{R}^{N\times N}$ are the left and right singular vectors, respectively. Because both $\mathbf{U}$ and $\mathbf{V}$ are unitary, we also have $\mathbf{U}\mathbf{U}^T = \mathbf{V}\mathbf{V}^T = \mathbf{I}$.

When the SDM is not reducible, exactly one of the singular values σ_i will be zero as a result of the fact that the loop filter displays a pole at DC. When the singular values are ordered in descending fashion, this singular value will be $\sigma_N = 0$. This has the interesting consequence, that the last column of $\mathbf{V}$ is a *non-relevant* direction, since it is always multiplied by $\sigma_N = 0$. This last column of $\mathbf{V}$ will be denoted $\mathbf{v}_0$ (the so-called null space of $\mathbf{I} - \mathbf{A}^P$: $(\mathbf{I} - \mathbf{A}^P)\mathbf{v}_0 = 0$). Now, if we know a single solution (say, $\mathbf{s}_{\mathrm{mn}}$) to Eq. (6), any solution $s^{(0)}$ can be expressed as:

$$\mathbf{s}^{(0)} = \mathbf{s}_{\mathrm{mn}} + \lambda\mathbf{v}_0 \tag{11}$$

In other words, the complete set of solutions to Eq. (6) is a *line*. We thus need to fulfill at least $N-1$ (initial) conditions for an N^{th} order SDM, in order to have a limit cycle.

In addition, the SVD is helpful in obtaining an initial solution to Eq. (6). First we have, similar to Eqs. (10,11), that:

$$(\mathbf{I} - \mathbf{A}^P)^T = \mathbf{V}\mathbf{\Sigma}\mathbf{U}^T; \qquad (\mathbf{I} - \mathbf{A}^P)^T\mathbf{u}_0 = 0 \tag{12}$$

where $\mathbf{u}_0$ is the null space of $(\mathbf{I} - \mathbf{A}^P)^T$. Therefore, Eq. (12) is equivalent to

$$\mathbf{u}_0^T(\mathbf{I} - \mathbf{A}^P) = 0 \tag{13}$$

Multiplying both sides of Eq. (6) with $\mathbf{u}_0^T$ we obtain

$$\mathbf{u}_0^T(\mathbf{I} - \mathbf{A}^P)\mathbf{s}^{(0)} = \mathbf{u}_0^T\mathbf{L}_P(\{y^{(i)}\}) = 0 \tag{14}$$

stating a necessary condition $\mathbf{u}_0^T\mathbf{L}_P(\{y^{(i)}\}) = 0$ for the existance of a solution to Eq. (6). For the type of SDMs that are investigated in this section, with a pole at DC (and thus infinite gain for DC) this condition is equivalent to the intuitively obvious condition that the average input should equal the average output of the SDM:

$$\frac{1}{P}\sum_{i=0}^{P-1} u^{(i)} = \frac{1}{P}\sum_{i=0}^{P-1} y^{(i)} \tag{15}$$

When the SDM input is a constant DC value, $u^{(i)} \equiv u$ and the sequence $\{y^{(i)}\}$ also completely determines the input u to the SDM.

Secondly, if a solution to Eq. (6) exists, we can define the *minimum norm* solution $\mathbf{s}_{\mathrm{mn}}$[3] to Eq. (6) as:

$$\mathbf{s}_{\rm mn} = \mathbf{V}\boldsymbol{\Sigma}'\mathbf{U}^T\mathbf{L}_P(\{y^{(i)}\});$$
$$\boldsymbol{\Sigma}' = \mathrm{diag}(\frac{1}{\sigma_1}, \frac{1}{\sigma_2}, \ldots, \frac{1}{\sigma_{N-1}}, 0) \quad (16)$$

The solution $\mathbf{s}_{\rm mn}$ is characterized by the fact that the norm $|\mathbf{s}_{\rm mn}|$ is the least of all norms $|\mathbf{s}^{(0)}|$ of other solutions to $\mathbf{s}^{(0)}$.

While we now have solved one part of the necessary conditions for a limit cycle, Eq. (6), we still have to solve for the set of inequalities represented in Eq. (9). For each inequality k in Eq. (9), we can write an equality which represents the conditions under which the constraint is on the edge of being violated:

$$(0,..0,1)[\mathbf{A}^k\mathbf{s}^{(0)} + \mathbf{L}_k(\{y^{(i)}\})] = 0 \quad (17)$$

This represents an $N-1$ dimensional hyperplane which bisects the N dimensional space. The point where this surface intersects the line defined by Eq. (11) represents the boundary where a limit cycle of length P is on the verge of violating the $k^{\rm th}$ constraint. This point is given by solving for $\lambda_k^{\rm crit}$ in the equation

$$(0,..0,1)[\mathbf{A}^k(\mathbf{s}_{mn} + \lambda_k^{\rm crit}\mathbf{v}_0) + \mathbf{L}_k(\{y^{(i)}\})] = 0 \quad (18)$$

This defines a distance $\lambda_k^{\rm crit}$ from the initial point $\mathbf{s}_{\rm mn}$ at which the $k^{\rm th}$ constraint is on the edge of being violated. Depending on the sign of $(0,..0,1)\mathbf{A}^k\mathbf{v}_0$, we need to have either $\lambda > \lambda_k^{\rm crit}$ (sign positive) or $\lambda < \lambda_k^{\rm crit}$ in order to fulfill the $k^{\rm th}$ constraint. We can now divide the set of constraints Eq. (18) into two categories:

$$\forall k = 0, ...P-1:$$
$$\text{if } (0,..0,1)\mathbf{A}^k\mathbf{v}_0 > 0, \text{ then } \lambda > \lambda_>^k = \lambda_k^{crit} \quad (19)$$
$$\text{if } (0,..0,1)\mathbf{A}^k\mathbf{v}_0 < 0, \text{ then } \lambda < \lambda_<^k = \lambda_k^{crit} \quad (20)$$

We can then define

$$\lambda_> = \max_k(\lambda_>^k) \quad (21)$$
$$\lambda_< = \min_k(\lambda_<^k) \quad (22)$$

which provides us with an interval $[\lambda_>, \lambda_<]$ for a feasible λ:

$$\lambda_{\rm feas} \in [\lambda_>, \lambda_<] \quad (23)$$

Obviously, when $\lambda_> > \lambda_<$, there is no feasible solution, and the limit cycle $\{y^{(i)}\}$ cannot exist.

3.2. No DC poles

A special situation arises when the SDM has no DC poles. In that case, the null space of $(\mathbf{I} - \mathbf{A}^P)$ is zero: there is only one solution $\mathbf{s}^{(0)}$ to Eq. (6). If this solution also complies with all inequalities Eq. (9), it results in a limit cycle. Because the null space is zero, any change of the integrator states would result in a break-up of the limit cycle. A relevant question that remains, however, is how long it would take before the bit-pattern is changed from the limit cycle pattern; in other words, what freedom do we have when the only requirement is to fulfill Eq. (9). This will be the subject of Sec. 4. Note, that the system of inequalities itself would lead to the same solution as Eq. (6) would after an infinite amount of time (see appendix 1).

3.3. Dither

Dithering, or adding random offsets to the quantizer, represents a special case of limit cycle disturbance, since it does not directly influence the integrator values. The only way in which dither can break up a limit cycle is by changing the sign of the input to the quantizer, causing it to create a bit-flip in the limit cycle output. As a result of that, a limit cycle will be broken up. The minimum amplitude $\nu_{\rm min}$ of the dither that is necessary to certainly break up a limit cycle, is easily determined as:

$$\nu_{\rm min} = \min_i \left| s_N^{(i)} \right|; \quad i = 0, ..., P-1 \quad (24)$$

thus the minimum dither level is dependent on the initial states. In a typical situation, where dither according to a certain (*e.g.*, rectangular) pdf spanning a width W is applied, all dither values with amplitude less than $\nu_{\rm min}$ are without any effect. Because of the dependence on initial states in Eq. (24), it is preferable to have an expression that provides the maximum of $\nu_{\rm min}$ over the initial states. The minimum amplitude dither $\nu_{\rm min}$, needed to break up a limit cycle, is maximised over all $\mathbf{s}^{(0)}$ when $\lambda = \frac{\lambda_< - \lambda_>}{2}$, and thus:

$$\nu_{\rm min} = \mathbf{v}_0 \frac{\lambda_< - \lambda_>}{2} \quad (25)$$

For most SDMs, the value $\nu_{\rm min}$ can be easily determined using results obtained previously, without resorting to Eq. (24). For SDMs without DC poles, however, the null-space has dimension zero and the methods outlined above cannot be used anymore. In this case, the only option is to determine the minimum amount of dither through Eq. (24).

4. STABILITY ANALYSIS OF LIMIT CYCLES

To determine whether a limit cycle is stable we will follow an approach to stability analysis based on perturbation theory. For a given limit cycle of length P, we can write for the states at clock cycle P:

$$\mathbf{s}^{(P)} = \mathbf{A}^P \mathbf{s}^{(0)} \tag{26}$$

To have some idea about stability of limit cycles, we will now disturb the original state variable $\mathbf{s}^{(0)}$ by an amount $\boldsymbol{\epsilon}^{(0)}$:

$$\hat{\mathbf{s}}^{(0)} = \mathbf{s}^{(0)} + \boldsymbol{\epsilon}^{(0)} \tag{27}$$

We have to investigate how such a disturbance propagates in time: whether it will get larger, or smaller in time. The growth of a disturbance $\boldsymbol{\epsilon}$ in the state variables after M periods (and, hence $n = MP$ clock cycles) of the limit cycle is given by:

$$\hat{\mathbf{s}}^{(MP)} = \mathbf{A}^{MP}(\mathbf{s}^{(0)} + \boldsymbol{\epsilon}^{(0)}) = \mathbf{s}^{(0)} + \boldsymbol{\epsilon}^{(MP)} \tag{28}$$

To analyze Eq. (28), we will create the Jordan decomposition [3] of $\mathbf{A}$, which is defined as[1]

$$\mathbf{A} = \mathbf{V}\mathbf{J}\mathbf{V}^{-1} \tag{29}$$

where $\mathbf{J}$ is a Jordan matrix of the form

$$J_{ij} = \begin{cases} \mu_i & \text{if} \quad i = j; \\ 0,1 & \text{if} \quad j = i-1; \\ 0 & \quad \text{otherwise}; \end{cases} \tag{30}$$

with μ_i the ith eigenvalue of the transition matrix $\mathbf{A}$. The main advantage of this decomposition is that it allows us to obtain a compact result of multiple application of $\mathbf{A}$ as

$$\mathbf{A}^k = \mathbf{V}\mathbf{J}^k\mathbf{V}^{-1} \tag{31}$$

where $J_{ii}^k = \mu_i^k$.

From this expression, we can immediately see that SDMs with eigenvalue magnitudes $|\mu_i| > 1$, multiple application of $\mathbf{A}$ will result in exponential growth of the disturbance. When $|\mu_i| < 1$, on the other hand, exponential decay will occur. The effect of a disturbance will be studied in the next sections, both for all eigenvalues $|\mu_i| = 1$, and for eigenvalues $|\mu_i| \neq 1$.

[1] Alternatively, the Schur decomposition could be used, which, for the types of SDMs under consideration, is less practical.

4.1. Only DC poles

In the special case where all the poles of the loop filter are at DC, all eigenvalues $|\mu| = 1$, as a result of which only polynomial growth can occur. In particular, when the eigenvalues are all unity, the result for $\mathbf{J}^n$ can be written as:

$$J_{ij}^k = \begin{cases} 1 & \text{if} \quad i = j; \\ 0 & \text{if} \quad i < j; \\ \begin{pmatrix} k \\ k-(i-j) \end{pmatrix} & \quad \text{otherwise}; \end{cases} \tag{32}$$

For a SDM with only DC poles, the transition matrix is exactly in the shape of this Jordan block, with eigenvalues equal to 1, and no further decomposition is necessary (SDMs which exhibit poles in the loop-filter, are not in Jordan form). In order to determine when a LC will be broken up, we have to determine the disturbance $\delta v^{(MP)}$ at the quantizer input that results in a bit-flip, akin to the discussion in Sec. 3.3. From Eq. (2), we have that

$$\delta v^{(MP)} = (0, ...0, 1)\mathbf{A}^{(MP)}\boldsymbol{\epsilon} \tag{33}$$

Using Eq. (32), making the approximation that $MP \gg 1$, and keeping only the highest terms, we can approximate the polynomial divergence of a modulator of order N

$$\delta v^{(MP)} \approx \epsilon_1 \frac{P^{N-1}}{(N-1)!} M^{N-1} + \epsilon_2 \frac{P^{N-2}}{(N-2)!} M^{N-2} + \vdots + \epsilon_N \tag{34}$$

where $\boldsymbol{\epsilon} = (\epsilon_1, \ldots, \epsilon_N)^T$.

Hence, if the first integrator is disturbed, the number of limit cycle periods M_c it takes before a limit cycle is broken up can be approximated by

$$M_c \approx \frac{1}{M}\left(\frac{(N-1)!|\delta v_{\text{crit}}|}{\epsilon_1}\right)^{1/(N-1)} \tag{35}$$

where δv_{crit} is the critical value of δv where the limit cycle is broken up. From Sec. 3.1, we have that

$$\delta v_{\mathrm{crit}} \in [\lambda_{>} - \lambda_{<}, \lambda_{<} - \lambda_{>}] \tag{36}$$

where the precise value of δv_{crit} depends on the initial state $\mathbf{s}^{(0)}$ and the coefficient vector $\mathbf{c}$ (Eq. (18)). This differs notably from the situation with feedforward sigma delta modulators, where the equivalent of Eq. (35) has an explicit dependence on the coefficients $\mathbf{c}$. For feedback SDMs, the dependence on coefficients is due solely to the $\mathbf{L}_k(\{y^{(i)}\})$ term in Eq. (18). Furthermore, unlike for feedforward designs, the nature of the dependence on the coefficients is not easily determined, since a change in the coefficients will affect the initial conditions which may result in a limit cycle, Eq. (6) as well as each constraint equation, Eq. (9). The effect of this difference is noticeable in the stability of limit cycles, which will be discussed in Sec. 5.2.

5. NUMERICAL RESULTS

The results of the work detailed in the preceding part, have been used to obtain some results on several different noise transfer functions (NTFs, all butterworth design), which have been implemented in feedback SDMs. The SDMs, are all fifth order with an oversampling ratio of 64, and have been chosen to illustrate the difference in behaviour for various SDMs with aggressive noise shaping and mild noise shaping. The naming convention is such, that the name of the SDM reflects its NTF corner frequency. For SDM120, the NTF has a -3 dB point at 120 kHz; for SDM80, this point is at 80 kHz. Thus, SDM80 represents a much less aggressive noise shaper than SDM120. They are all of the type displayed in Fig. 1.

In the following sections, we will discuss results on static and dynamic behaviour of SDMs. Feedback topologies are presented to judge how the implementation topology influences the limit cycle behaviour.

5.1. Static behaviour

In [12, 13], the authors presented a variety of results which depicted the occurrence of limit cycles for a variety of feedforward sigma delta modulators. The results for the equivalent feedback designs are not presented here because they are virtually identical.

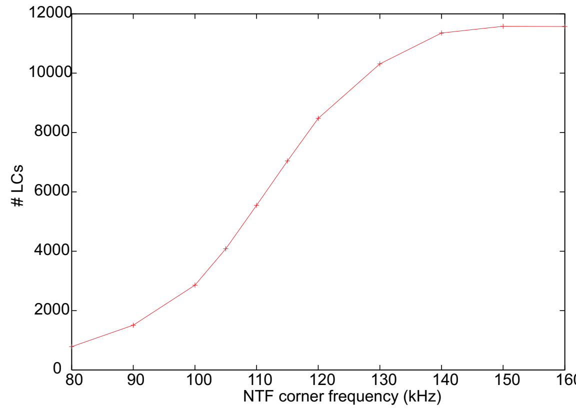

Fig. 2: *Number of limit cycles for a fixed LC period of 24, as a function of the NTF corner frequency used in the SDM design.*

This is because the equations for limit cycle existence, Eq. (6) and Eq. (9), differ from their feedforward equivalents only in the placement of the coefficient vector $\mathbf{c}$ and its replacement with $(1, 0, ...0)^T$. The transition matrix, however, is unaffected. As we shall see, this affects how a limit cycle may be broken up (either the dither level required, or the time until a disturbance leads to a bit flip), but has little effect on limit cycle existence or stability.

The dependence of the number of LCs at given LC length ($P = 24$) on the corner frequency of the butterworth NTF design is given in Fig. 2. This clearly illustrates the increase of the number of limit cycles with increased aggressiveness of the SDM, and also shows that for highly aggressive SDMs the number of possible LCs is virtually constant. The figure is almost identical to one published in [12]. This indicates that the number of limit cycles of a given period, although strongly dependent on noise shaping characteristics, is virtually independent of the choice of feedforward or feedback design.

In Fig. 3, the minimum dither level that is needed to certainly break up the most stable limit cycle is depicted. The limit cycles for the aggressive SDM 120 are *more stable* against dither than those of the less aggressive SDM 80. This is counter-intuitive since we expect aggressive SDMs to be less susceptible to limit cycles. Also, we can see that there is a very stable limit cycle occurring around LC length 22 for SDM 120, and for LC length 32 for SDM 80.

Upon investigation of these limit cycles, it appeared that they consist of a series of 11 1s followed by 11 -1s for SDM 120, and likewise 16 1s and 16 -1s for SDM 80. This corresponds to a square wave of frequency 120 kHz and 80 kHz, respectively, which are exactly the corner frequencies of the NTF design of the SDMs. Although not shown, identical behaviour occurs for other SDMs. In practice, however, these LCs require huge initial integrator states that could never occur: long before such an integrator state could be reached in real operation, the SDM would have gone unstable. As a result, if the SDM has been forced into this limit cycle, the SDM runs unstable upon the slightest disturbance of the integrators.

Again, these results are quite similar to those found for feedforward designs and presented in [12]. The very stable limit cycles occur at the same limit cycle lengths, and the general trends observed are the same. The minimum dither levels differ between the two design methods principally due to the fact that the coefficient vector has a different effect on the quantiser input value for each design.

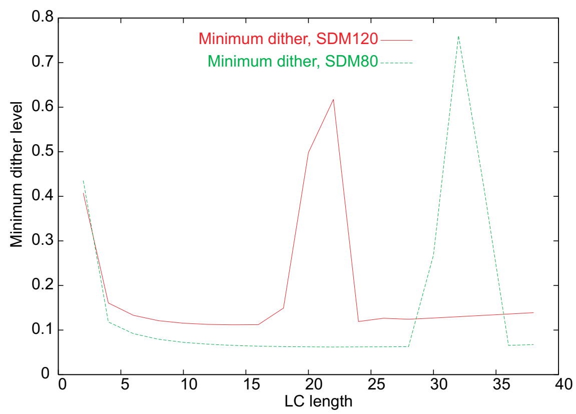

Fig. 3: *Minimum level of dither needed to break up the most stable limit cycle corresponding to a DC input 0 .*

This is to be contrasted with the LC behaviour for other LC lengths. The shortest LC, the sequence $\{1, -1\}$, appears to be most stable (disregarding the previously discussed LCs) for both SDMs. For longer LCs, the amount of dither needed for break-up decreases to a minimum value close to the peak, after which the LC becomes more stable. All these limit cycles consist of the sequence $\{-1, 1, -1, 1, \ldots, -1, 1, -1, -1, 1, 1\}$, which represents the minimally possible deviation for the simple $\{-1, 1\}$ sequence. While these most stable limit cycles slightly increase in stability for longer LCs, on average the amount of dither necessary for break-up decreases. Again, we see that SDM 120 presents LCs that are in general more stable than those of SDM 80.

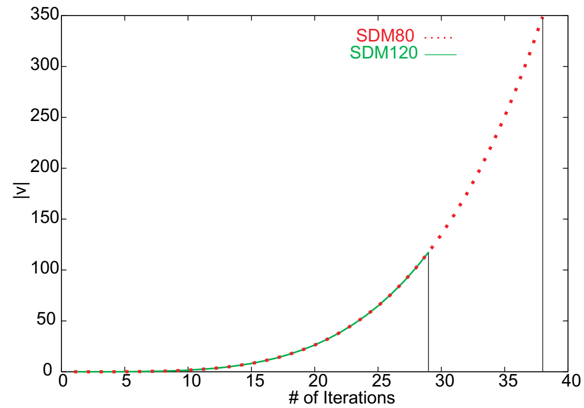

Fig. 4: *Disturbance of identical limit cycles (most stable period 8 limit cycle) for SDM 120 and 80, with all eigenvalues equal to 1, due to a small disturbance (-120 dB) on the first integrator state. Depicted is the quantizer input until the limit cycle breaks up. The vertical lines give the number of iterations at which the limit cycle is broken.*

5.2. Dynamic behaviour

In Fig. 4, the effect of a small disturbance of the integrator states on a limit cycle is illustrated. In Fig. 4 we plot the quantity $|\delta v|$, which is the deviation of the quantizer input from its ideal input, such as defined in Eq. 33. The limit cycle studied was the most stable of length 8, *i.e.*, $-1, -1, +1, +1$ followed by a sequence of 2 $-1, +1$ pairs. A disturbance of -120 dB (10^{-6}) was applied to the first integrator at time instant $n = 0$ in order to break up the limit cycle. The effect of such a disturbance on the output signal is very small; in fact, it is much less than the effect that sufficiently dithering the quantizer would have had. However, the behavior is noticeably different from that which occurs for the feedforward design. We can clearly see that for both the mild and aggressive noise shapers, the growth rate of a disturbance is the same. However, for SDM120, which is the more aggressive one, the limit cycle is broken up after only 29 periods, whereas the same limit cycle for SDM80 is broken up after 38 limit cycles.

This is to be contrasted with feedforward designs, where the growth of the disturbance at the quantiser input may vary with different noise shapers[12, 13]. The reason for this difference is that the feedback coefficients in a feedback design only represent a constant shift of the integrator states, and thus can affect when a bit flip occurs, but not the growth of a disturbance. Whereas, for feedforward designs, the coefficients represent a multiplier that is applied directly to the quantiser input, and thus affect its growth rate. Interestingly, the number of limit cycle periods before break-up occurs hardly differs between feedback and feedforward designs[12, 13]. Apparently, even though the dynamics of a feedback SDM appear to be different from that of a feedforward design, the results are virtually identical.

Results are not presented here for designs with resonator sections or other modifications of the transition matrix. This is because the derivation and simulation of dynamic behavior of these systems exactly parallels the results in [13] for feedforward SDMs. There, it was shown that very small changes in an SDMs structure can have significant effects on the rate of growth of any disturbance to a limit cycle. SDMs with only DC poles will exhibit polynomial growth, whereas the inclusion of resonator sections or other modifications to the feedback/feedforward structure will exhibit exponential growth. However, if these modifications result in the transition matrix having complex conjugate pair eigenvalues, then the exponential growth is exhibited as the disturbance *spiraling* away from initial conditions. Thus, this exponential growth may actually take significantly longer to break up the limit cycle than the polynomial growth which occurs without resonators. Therefore, in general, SDMs without resonators are less susceptible to limit cycles. Details of these results are provided in [13] .

6. CONCLUSIONS

This work is an attempt to construct a general theory describing limit cycles in 1-bit feedback sigma delta modulators, and to provide the designer with tools other than numerous simulations to obtain an insight into typical limit cycle behaviour of SDMs. The work parallels results already established for feedforward SDMs, and many equivalent conclusions are established. It has been proven that, under almost all circumstances, limit cycle behaviour is observed in the output if and only if a limit cycle occurs in state space. It has been shown that limit cycle behaviour can occur in a wide variety of situations.

In Section 3.1, a recipe was given whereby, for constant input, *all* limit cycles of a given period can be found for any feedback SDM with at least one pole at DC. Eq. (16) provides a least squares solution to the limit cycle conditions. If the constraint equations, Eq. (9) and Eq. (15), are satisfied, then this is an exact solution. Eq. (18) may then be solved to find the exact set of initial conditions, Eq. (11), which give rise to this limit cycle. When the SDM has no DC poles, this procedure becomes simpler since Eq. (6) can be solved directly and Eq. (9) is the only constraint. The essential difference between these situations is that, if constraint equations are satisfied, SDMs with DC poles will exhibit a line of initial conditions which give rise to a limit cycle, whereas SDMs without DC poles will exhibit a unique solution. One consequence of the initial condition dependence is that, for an SDM of order N with DC poles, $N-1$ states need to have a well-defined value, and all N states need to have a well-defined value for SDMs without DC poles. This makes limit cycles for higher order SDMs (which typically exhibit more aggressive noise shaping) less likely to occur, especially when they do not exhibit poles at DC.

It has also been shown that dithering the quantizer is not the optimal way of removing limit cycles: adding a small disturbance to an integrator state is far more efficient and will always result in break up of the limit cycle. The noise penalty is rather limited, as the input disturbance can be made as small as 10^{-6} or -120 dB.

An important characterisation given the goals of SDM design, is distinguishing limit cycle behaviour for SDMs with different noise shaping characteristics. SDMs with aggressive noise shaping can sustain many more different limit cycles than SDMs (of equivalent order) with mild noise shaping, and are more robust against dithering the quantizer. Though the number of limit cycles grows exponentially, limit cycles of a long period are more sensitive to a small disturbance than short limit cycles. Likewise, SDMs with aggressive noise shaping are more sensitive to disturbances than mildly noise shaped SDMs - even though the latter exhibit a much smaller number of sustainable limit cycles. This is corroborated by the experimental observation that aggressive noise shapers are less susceptible to limit cycles than mild noise shapers.

Though the derivation of these results differs from the derivation for feedforward SDMs, the conclusions are the same. However, the exact number of limit cycles, and their locations in state space, may differ slightly between the two designs. Furthermore, the growth rate of a disturbance is dependent on the feedforward coefficients for feedforward SDMs, whereas the growth rate of a disturbance to a limit cycle in a feedback SDM has *no dependence* on the feedback coefficients. The dependence on coefficients is exhibited in the minimum dither level, or size of a disturbance, required for a limit cycle to be broken up. In general, the choice of feedback or feedforward sigma delta modulators was not found to provide any significant advantage or disadvantage in terms of limit cycle behavior.

1. PROOF THAT THE EQUALITIES ARE A SUFFICIENT CONDITION FOR A LIMIT CYCLE

In this appendix, we will prove that the set of inequalities Eq. (9) leads to the same solution as the set of equalities Eq. (6) would, *i.e.*, whether the limit cycle condition observed at the output of the SDM:

$$y^{(n+P)} = y^{(n)} \tag{37}$$

leads to the limit cycle condition as known in stability analysis:

$$\mathbf{s}^{(n+P)} = \mathbf{s}^{(n)} \tag{38}$$

For example, if the output sequence happens to be a periodic sequence of period P, one could ask the question whether there exists a possibility that an initial state $\mathbf{s}_0$ does not return to this value after propagation over P cycles, but to a different state vector $\mathbf{s}'$. If this state vector generates the same output sequence again, *etc.*, we have a limit cycle without fulfilment of Eq. (6). To that end, we look at the propagation of the state variables Eq. (4), after a large number NP of cycles. We will further assume that $(\mathbf{I}-\mathbf{A}^P)$ is invertible; when it is not we will define a new transition matrix $\tilde{\mathbf{A}}$ as

$$\tilde{\mathbf{A}} = \mathbf{A}' + \epsilon\mathbf{I} \tag{39}$$

where $\mathbf{A}'$ is the original transition matrix, and $\mathbf{I}$ is the unit matrix. Now $(\mathbf{I}-\tilde{\mathbf{A}}^P)$ is invertible by definition; at the end of the analysis we will than have to take the limit $\epsilon \to 0$ to obtain the final result.

From Eq. (4), we subsequently determine the states $\mathbf{s}^{(NP)}$ at the NPth clock cycle as:

$$\mathbf{s}^{(NP)} = \tilde{\mathbf{A}}^{NP}\mathbf{s}^{(0)} + \sum_{i=0}^{NP-1} \tilde{\mathbf{A}}^{NP-i-1}(u^{(i)}\mathbf{d} - y^{(i)}\mathbf{c}) \tag{40}$$

The summation can be written as two nested summations:

$$\mathbf{s}^{(NP)} = \tilde{\mathbf{A}}^{NP}\mathbf{s}^{(0)} + \sum_{j=0}^{N-1}\sum_{i=0}^{P-1} (u^{(i)}\mathbf{d} - y^{(i)}\mathbf{c})\tilde{\mathbf{A}}^{NP-(jP+i)-1} \tag{41}$$

where we used the fact that $\{y^{(i)}\}$ is a limit cycle and $\{u^{(i)}\}$ is constant, i.e., $u^{(i+P)}\mathbf{d} - y^{(i+P)}\mathbf{c} = u^{(i)}\mathbf{d} - y^{(i)}\mathbf{c}$.

The terms not dependent on i can be moved outside the summation:

$$\mathbf{s}^{(NP)} = \tilde{\mathbf{A}}^{NP}\mathbf{s}^{(0)} + \sum_{j=0}^{N-1}\tilde{\mathbf{A}}^{jP}\sum_{i=0}^{P-1} (u^{(i)}\mathbf{d} - y^{(i)}\mathbf{c})\tilde{\mathbf{A}}^{P-i-1} \tag{42}$$

Because the sum over i represents a constant, we define

$$\mathbf{L}_P(\{y^{(i)}\}) = [\sum_{i=0}^{P-1}(u^{(i)}\mathbf{d} - y^{(i)}\mathbf{c})\tilde{\mathbf{A}}^{P-i-1}] \tag{43}$$

in line with earlier definitions in Sec. 2.2. With this definition, we can write Eq. (41) concisely as:

$$\mathbf{s}^{(NP)} = \tilde{\mathbf{A}}^{NP}\mathbf{s}^{(0)} + \sum_{j=0}^{N-1}\tilde{\mathbf{A}}^{jP}\mathbf{L}_P(\{y^{(i)}\}) \tag{44}$$

Realizing that the finite sum represents a geometric series, and because we have defined $\tilde{\mathbf{A}}$ such, that

$(\mathbf{I}-\tilde{\mathbf{A}}^P)$ is by definition invertible, Eq. (44) can be expressed as follows:

$$\mathbf{s}^{(NP)} = \tilde{\mathbf{A}}^{NP}\mathbf{s}^{(0)} + (\mathbf{I}-\tilde{\mathbf{A}}^{NP})(\mathbf{I}-\tilde{\mathbf{A}}^P)^{-1}\mathbf{L}_P(\{y^{(i)}\}) \quad (45)$$

For convenience, we will further define

$$\mathbf{r} = (\mathbf{I}-\tilde{\mathbf{A}}^P)^{-1}\mathbf{L}_P(\{y^{(i)}\}) \quad (46)$$

due to which we can further compress Eq. (44) as

$$\mathbf{s}^{(NP)} = \tilde{\mathbf{A}}^{NP}(\mathbf{s}^{(0)}-\mathbf{r})+\mathbf{r} \quad (47)$$

In order for a limit cycle to be stable, $\lim_{N\to\infty}|\mathbf{s}^{(NP)}|$ must be bounded. We will discriminate two cases.

Case 1: $(\mathbf{s}^{(0)}-\mathbf{r})$ corresponds to eigenvalues with norm larger than 1

If $(\mathbf{s}^{(0)}-\mathbf{r})$ contains directions which correspond to eigenvalues with a norm larger than 1 of $\tilde{\mathbf{A}}$, $\lim_{N\to\infty}|\mathbf{s}^{(NP)}|$ is bounded *only* when:

$$\mathbf{s}^{(0)} = \mathbf{r} \quad (48)$$

leading to

$$\mathbf{s}^{(NP)} = \mathbf{s}^{(0)} \quad (49)$$

which is the conjecture on which the results in Sec. 2.2 are based.

Upon applying the definition of Eq. (39) to Eq. (47), we see that we can safely take $\lim_{\epsilon\to 0}$ by setting $\epsilon = 0$, as a result of which Eq. (48) is independent of the invertibility of $(\mathbf{I}-\mathbf{A})$. The definition of $\mathbf{r}$ in Eq. (46) also turns out to be a familiar result, as with $\mathbf{r} = \mathbf{s}^{(0)}$ it is identical to Eq. (7) in Sec. 2.2.

Case 2: $(\mathbf{s}^{(0)}-\mathbf{r})$ corresponds to eigenvalues with norm smaller than 1

If, on the other hand, $(\mathbf{s}^{(0)}-\mathbf{r})$ contains only directions which correspond to eigenvalues < 1 of $\tilde{\mathbf{A}}$, these directions will be reduced to zero if $\lim_{N\to\infty}$. We thus obtain as a result

$$\mathbf{s}^{(NP)} = \mathbf{r} \quad (50)$$

which is identical to Eq. (48) when $\mathbf{s}^{(NP)} = \mathbf{s}^{(0)}$. However, we do not have the result that $\mathbf{s}^{(NP)} = \mathbf{s}^{(0)}$. Thus, in this case, we have a possibility that an initial state $\mathbf{s}^{(0)}$ does not return to this value after propagation over P cycles, but to a different state vector $\mathbf{s}'$, and that this state vector generates the same output sequence again. After a long number of limit cycle periods, however, $\mathbf{s}^{(NP)}$ converges to a unique value, such that $\mathbf{s}^{(NP)} - \mathbf{s}^{((N+1)P)} = 0$ which is a situation identical to Case 1.

2. REFERENCES

[1] S. R. Norsworthy, R. Schreier, R. and G.C. Temes, Delta Sigma Converters, Theory, Design and Simulation, IEEE Press, New York, 1997

[2] A. V. Oppenheim, and A. W. Shafer, Discrete Time Signal Processing, Prentice-Hall, Englewood Cliffs, NJ, 1989

[3] G. H. Golub, and C. F. Van Loan, Matrix computations, 3rd Edition, The Johns Hopkins University Press, Baltimore and London, 1996

[4] S. Hein, and A. Zakhor, Sigma Delta Modulators: nonlinear decoding algorithms and stability analysis, Kluwer Academic Publishers, New York, 1993

[5] D. Hyun, and G. Fischer, Limit cycles and pattern noise in single-stage single-bit delta-sigma modulators, IEEE Trans. Circuits and Systems I, vol. 49, pp. 646-656, 2002

[6] F. de Jager, Delta modulation - a method of PCM transmission using the one unit code, Philips Res. Rep., vol. 7, pp. 442-466, 1952

[7] A. J. Magrath, Algorithms and Architectures for High resolution Sigma-Delta converters, PhD Thesis, University of London, 1996

[8] L. Risbo, Sigma-delta modulators: stability analysis and optimisation, PhD Thesis, Technical university of Denmark, 1994

[9] D. Reefman and P.A.C.M. Nuijten, Editing and Switching in 1-bit audio streams, Proceedings of the AES 110th convention, preprint 5399, 2001 May 12-15 Amsterdam, 2001

[10] S. H. Ardalan, and J.J. Paulos, An Analysis of Nonlinear Behavior in Delta-Sigma Modulators, IEEE Transactions on Circuits and Systems, vol. CAS-34, pp. 593-603, 1987

[11] D. Reefman and E. Janssen, White paper on Signal processing for SACD, Philips IPandS, Eindhoven, 2003

[12] D. Reefman, J. D. Reiss, M. Sandler and E. Janssen, Stability Analysis of Limit Cycles in High Order Sigma Delta Modulators, Proceedings of the Audio Engineering Society 115th Convention, New York, New York, 2003.

[13] D. Reefman, J. D. Reiss, M. Sandler and E. Janssen, Description of limit cycles in Sigma Delta Modulators, submitted to IEEE Transactions on Circuits and Systems, pp. 30, 2004.