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Idle tone behavior in Sigma Delta Modulation

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ABSTRACT

This paper examines the relationship between various unwanted phenomena that plague audio engineers in the design of Sigma Delta Modulators. This work aims to clarify the difference and relationship between single DC idle tones, long limit cycles, short limit cycles and 'periodic' short limit cycles, while extending the current knowledge in idle tone behavior. A relationship between the periodic input to the quantizer of a 1-bit Delta Sigma Modulator and the appearance of idle tones is shown. It is shown that for a large range of input signal magnitudes, the fundamental frequency of idle tones is proportional to the DC input. This finding has also been used to examine idle tone aliasing. Numerous simulations are reported which confirm these findings.

1. INTRODUCTION

Currently Sigma Delta Modulators (SDMs) are one of the most popular designs for audio data acquisition. SDMs are common in audio Analog to Digital (ADC) and Digital to Analog (DAC) converters. Other uses of sigma delta modulators include data coding in Super Audio Compact Disc (SACD) and Direct Stream Digital (DSD). A SDM in its simplest form is a feedback system consisting of an integrator and quantizer. In a SDM, the feedback serves as a mean of reducing the quantization error. The integrator stage usually consists of a Low Pass Filter (LPF), and the quantizer is a comparator. The quantizer can be of two types; one-bit or multi-bit. In the multi-bit case the quantizer consists of a comparator array. A SDM schematic can be seen in Figure 1.

It is important to understand that due to the non-linear nature of the quantizer, together with the feedback design, SDMs can introduce audible undesired artifacts during the conversion process. The behavior of two of the most commonly encountered effects of non-linearity, idle tones and limit cycles, will be the central focus of analysis in the following research.

The terms idle tone and limit cycles are two of the most misunderstood and often misused or interchanged terminologies in SDM theory. In some cases limit cycles have been referred to as a subset of idle tones [1]

and several classifications have been attempted [2]. This paper will attempt to classify and explain these phenomena, as well as extend current understanding of them.

One of the most accepted definitions of limit cycles is that a limit cycle is "a sequence of *P* output bits, that repeats itself indefinitely"[3]. Results provided by this research will show that the definition is accurate, but it does not fully account for several other related and observed phenomena, e.g. short limit cycles. While limit cycles are fairly well understood, and their behavior can be mathematically explained by the use of state space equations [4], idle tones remain less understood. Idle tones are the appearance of undesired partials in the spectrum, which were not present in the input signal. By partials, we mean a constituent frequency, which is not necessarily an integer multiple of a fundamental frequency, which can be identified above the noise floor. A more precise definition on idle tone phenomena will be stated in section 4.4 of this paper.

This research will concentrate on the study of one-bit SDMs with DC inputs only. Although there may exist undesired audio artifacts with one-bit SDMs used for high quality audio applications [5], this work is concerned solely with the study of the behavior of these undesired artifacts. Therefore, the SDMs used herein are implemented without dither or any other corrective technique to avoid limit cycles or idle tones.

2. THE EXPERIMENTAL SETUP AND PROCEDURES

One common method for studying non-linear phenomena in SDMs is the use of synchronous averaging. In some cases synchronous averaging of the data is needed for the artifacts caused by idle tones to become visible in spectral plots. The existence of partials buried within the noise-floor can be thought as the convolution of a random signal with a partial. This will result in a random sequence with the same spectrum as the original random noise [6]. For this reason, noise shaping and idle tones can coexist together. In some cases idle tones can be audible but not visible in a spectrum. If a synchronous averaging is performed and proper windowing is performed [1], they can become visible.

A second method for studying non-linear phenomena in SDMs is to perform extremely long FFTs, which usually are inefficient and time consuming. It can be argued that this method is more representative of realistic signals, since there is no music or speech audio signal which will be repetitive enough to comply with a synchronous averaging method. For this reason the method of performing very long FFTs has been used for obtaining the results in this paper.

Unless otherwise noted, all simulations were performed for one second at 64 times oversampling (*OSR*=64) for a 44.1kHz Nyquist rate (F_h=44.1KHz) and a sampling frequency of (f_s=64x44.1kHz=2.8224MHz). Simulating the SDM for one-second periods gives the possibility to relate the input of the quantizer data to the frequency of the idle tone in terms of cycles per second in a straightforward manner. Measurements were taken by a variable resolution FFT software. The resolution of the measurement varies according to the time domain area to be studied. The FFT uses a single Hann window over all data before performing the FFT. This means that for the cases where the FFT was done over a whole simulated data set, a 1 Hz resolution was achieved. This setup permits an arbitrary zooming into any even starting and end point of the time domain generated data. Where needed, the FFT data has been padded with zeros. The FFT measurements were done at the output of the SDM *O(t)*. Time domain measurements of the input of the quantizer $Q_{in}(t)$ were also performed.

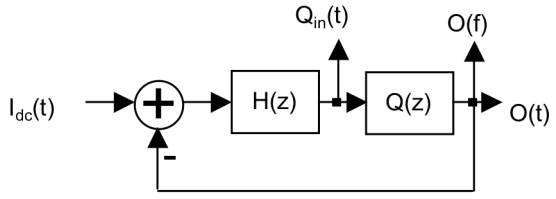

Figure 1 General schematic of a SDM. $I_{dc}(t)$ represents input, *O(t*) represents output, *H(z)* the integrator stage and *Q(z)* the quantizer. Measurement points are denoted as $Q_{in}(t)$, the time domain input to the quantizer and *O(f)*, the output spectrum of the SDM.

A block diagram of the SDM showing where the time domain and spectral measurements were taken is shown in Figure 1. Simulations were performed on SDM designs based on. Schreier's toolbox[7] or described in Reefman et al. [8]. The SDM coefficients used to obtain the plots presented in this paper are detailed in the appendix A.

In the following two sections, a series of experimental test results will be given in order to show the broad range of different limit cycle and idle tone phenomena that may be exhibited by the SDMs under investigation.

3. LIMIT CYCLES

Limit cycle behavior is an undesired phenomenon which, in this case, results from the feedback around the nonlinearity. All limit cycles are highly dependent on initial conditions. Contrary to linear filter design theory, careful placement of poles and zeros in SDM design does not typically result in limit cycle avoidance [9]. Dithering [6] and other methods, like bit flipping methods [10] or the more efficient mechanism described in [11], have proven to be effective in removing limit cycles. This section is concerned with studying and classifying the limit cycle-related phenomena rather than their removal.

A limit cycle can be defined as when the SDM output bit stream becomes cyclical and enters a repetitive pattern. This represents the standard well-known behavior of limit cycles. In this sense the SDM becomes a square wave generator which results in a set of well define harmonics with no noise shaping. As explained in [12] it results in a series of harmonics which can be related to the square wave pattern of the SDM output. It is important to notice that the existence of a fixed repetition of a sequence of bits means that no noise shaping is to be expected.

Based on a 5th order SDM design with an 80Hz corner frequency (see Appendix A), with initial conditions set to zero and a DC input of 0V, a limit cycle was generated. The input to the quantizer, shown in Figure 2, is in a repetitive sequence. This sequence remains the same from start to finish for a one-second simulation. The same can be said of the data sequence obtained at the output of the SDM. This complies perfectly with the definition that a limit cycle must be a sequence that repeats indefinitely.

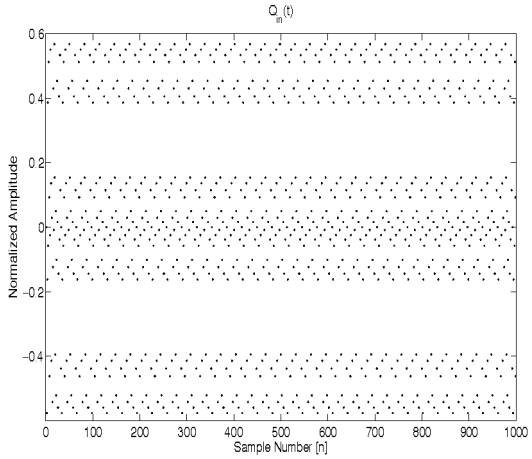

Figure 2 Time domain plot of the input to the quantiser during a limit cycle.

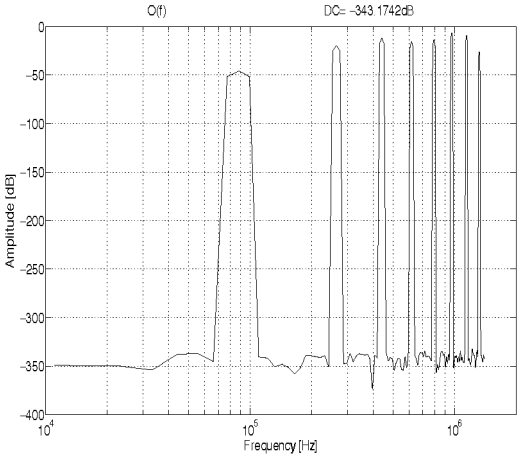

Figure 3 Spectrum of the quantiser output bitstream during a limit cycle (samples 256 to 512).

Figure 3 plots 256 samples of the output of the SDM. It can be seen, that it complies with the concept of having no noise shaping.

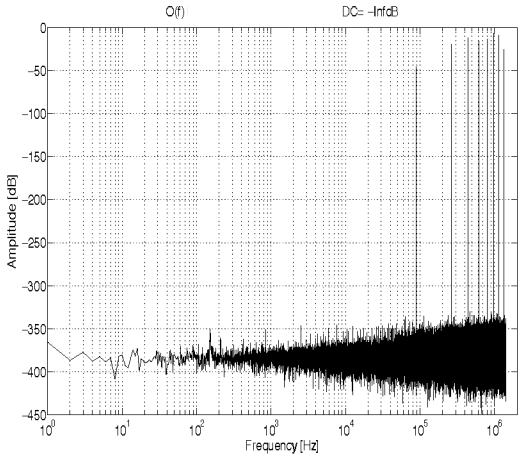

Figure 4 Spectrum of the quantiser output bitstream during a limit cycle (1 second, FFT resolution 1Hz).

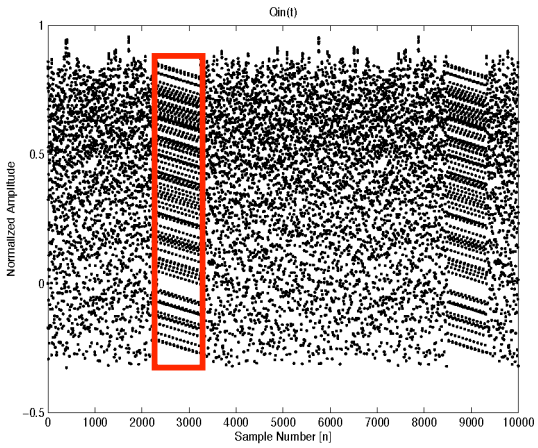

Figure 5 The input to the quantiser in the time domain, containing a short limit cycle in the enclosed rectangle.

The spectral plot of the limit cycle for one second of data is shown in Figure 4. It can be seen that the partials due to the limit cycle are the same if the output of the SDM is studied either for a few samples, as in Figure 3, or for a longer period of time. Effectively it does not contain noise shaping, but it does contain some amount of white noise due to finite data size and due to quantization errors. The presence of white noise should average to zero if an FFT is performed for an infinite period of time.

3.1. Short Limit Cycles

For this test, the same SDM was used as in the previous section, with initial conditions set to zero and a DC input of 0.7V. The first input sample (X_{in0}=0) was forced to be zero. Figure 5 depicts the input of the quantizer of the SDM. Isolated stripes of sequenced data may be observed. This accounts for a limit cycle condition, which only occurred for a limited time before reentering an unstructured pattern representing normal operation. The isolated stripes are a typical pattern of a short limit cycle.

Data contained inside the short limit cycle follows a periodic wave shape, resulting in a fully periodic output bitstream with a period length of 80 samples. On the other hand, this short limit cycle, as a unit, contained inside the square in Figure 5, is aperiodic, at least during the one second studied. It does not reoccur at periodic intervals, though it does occurs again atleast 4 times (at samples $8.522\text{x}10^3$, $6.269\text{x}10^5$, $1.731\text{x}10^6$, and $2.654\text{x}10^6$). Evidence of short limit cycles may also be seen at other times, e.g. $8.923\text{x}10^4$seconds, though these are most likely different limit cycles. In all cases studied during this research, the limit cycle seems to stop every time the input to the quantizer data reaches a value close to zero and the output bitstream is broken.

The short limit cycle occurs for a finite period of time because the state space variables, or integrator values, approach the limit cycle but are not on the exact values which would give limit cycle behavior indefinitely. Thus, they drift in the vicinity of the limit cycle with a repeating output bit sequence, until eventually they diverge far enough away from the limit cycle for an output bit to be flipped and normal behavior resumes.

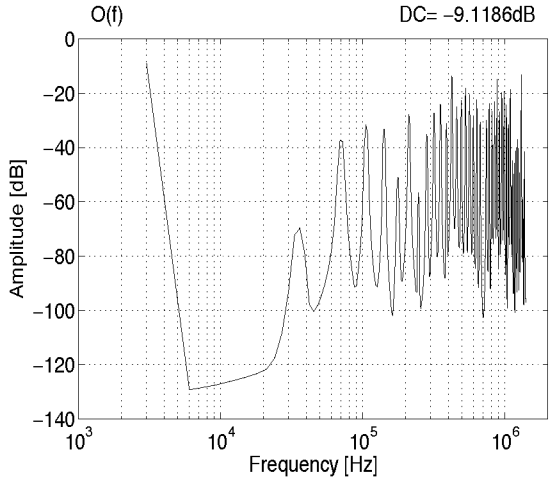

Figure 6 Spectrum of the output bitstream during a short limit cycle (samples 2304 to 3242).

A series of 938 samples of the output of the SDM corresponding to the short limit cycle are shown in Figure 6. The samples correspond in time to one of the striped sequences of data present at the input of the quantizer in Figure 5. A short limit cycle can occur for finite periods of time even when the input signal is constant for all time.

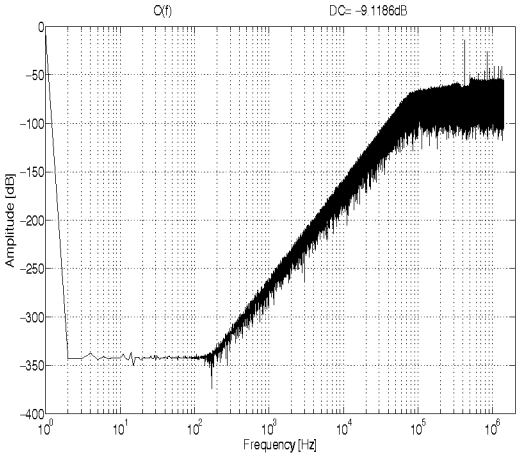

Figure 7 Short Limit Cycle Spectrum (1 minute FFT resolution 1Hz)

In Figure 7 we can observe the output spectrum of this SDM over a duration of one second. Because no synchronous averaging has been used and the short limit cycle is quite brief in time (938samples) the effect of short limit cycles cannot be seen in a simple spectral plot. The lack of a simple spectral relationship to the time domain evidence of limit cycles, together with the convenience of state space analysis has lead researchers in this field to speak of limit cycles as a time domain problem rather than a frequency domain phenomenon [9]. The partials at the top right part of the plot are idle tones and will be explained in detail in section 4. For a short limit cycle it can be said that it is a short, isolated repetitive sequence of data.

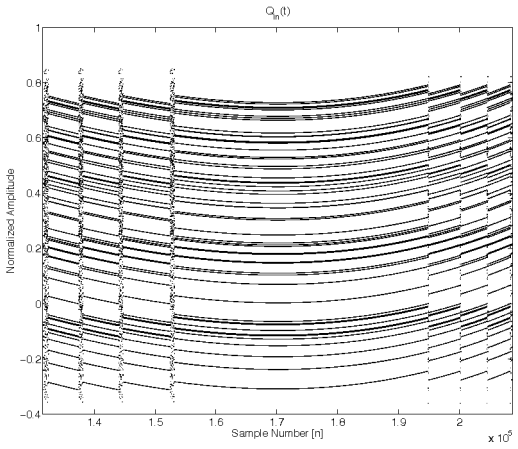

Figure 8 Time Varying Short Limit Cycle (Time Domain for samples 1.37200×10^5 to 2.08600×10^5).

Using the same SDM a series of short limit cycles can be obtained with a DC input of 0.6, shown in Figure 8. In this case the duration of the limit cycle first increases in length and then decreases in length. This may be explained because each time the limit cycle is broken it is then reentered closer or further away from the exact integrator state values which would result in a normal limit cycle (as in Fig. 3). Thus the divergence results in longer or shorter number of repetitions of the short term limit cycle before it is broken up.

3.2. Periodic Limit Cycles Observations

In this section, the same SDM was used, with initial conditions set to zero and a DC input of 0.5V.

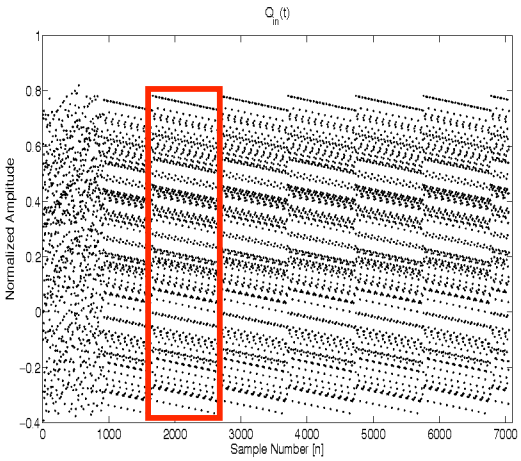

Figure 9 Periodic Limit Cycle (Time Domain)

The start of a periodic limit cycle is shown in Figure 9. Here, there is an initial transient stage, without periodic behavior. Then, a limit cycle forms until an output bit in the cycle is flipped. However, at this point it reenters the same limit cycle and repeats the pattern. This periodic short term limit cycle behavior remains for the rest of the simulation.

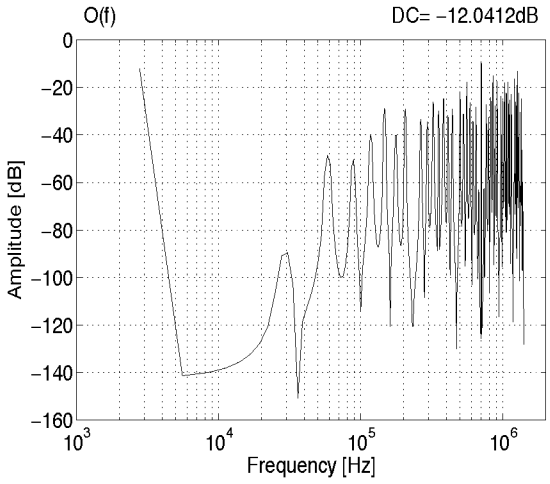

Figure 10 Output spectrum of a periodic short term limit cycle (samples 1667 to 2683).

The spectral plot of 1016 samples of the output of the SDM, which corresponds in time to one of the diagonal stripes of data in the input to the quantizer, is presented in Figure 10. As can be seen here, the sequence at the output of the SDM does contain some amount of noise shaping. This is contrary to what is to be expected based on the non-noise shaped behavior exhibited in a normal limit cycle.

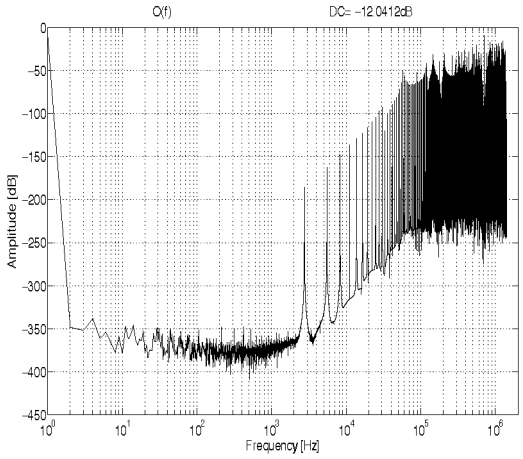

Figure 11 Periodic Limit Cycle Spectrum (1 second FFT resolution 1Hz)

There are two periods of note in this example, one corresponding to the length of the bitstream sequence, and the other to its duration before a bit is flipped and the system reenters the short limit cycle. The bitstream sequence has a period of 96 samples, and the SDM is in this limit cycle over 1016 samples before the short limit cycle is broken and then reentered. The larger period of 1016 samples corresponds to approximately 2778 repetitive attempts per second to enter into a limit cycle. This also represents the frequency of the first partial found in Figure 11.

3.3. Limit Cycles Observations

Limit cycles are an undesired phenomenon related to non-linearitys and feedback design, in which the output bitstream of the SDM gets locked permanently or for a given period of time in a repeatable sequence. They can be easily identified by the appearance of well-defined vertical stripes of data at the input of the quantizer. This repeatable sequence causes the SDM to act as an oscillator. It will result in a series of spectral components which are free from noise shaped noise. If the integrator states of an SDM are near the states required for an indefinitely repeating limit cycle, it may result in related phenomena, such as short term limit cycles or periodic short term limit cycles. In these situations, some noise-shaping may be evident along with unwanted partials in the output spectrum. In these

cases, since the partials are due to a repeating bitstream pattern, they are harmonically related.

4. IDLE TONES

Idle tones are an unwanted phenomenon, which is mainly associated with the appearance of partials in the SDM output spectrum that were not in the original input signal. It remains one of the less understood SDM behaviors. When idle tone are in the audible range of the spectrum and their magnitude is bigger than the audible human threshold they can become audible.

It was found during this research that the shape of the input to the quantizer data is directly related to the spectral appearance of DC idle tones of the SDM. The typical appearance of an idle tone is plotted in Figure 12. This plot has been taken from the time domain data to the input of the quantizer. A modified version of Reefman's 5th order SDM design (see Appendix A) with an 80Hz corner frequency, with initial conditions set to zero and a DC input of 0.000354308390023V was used.

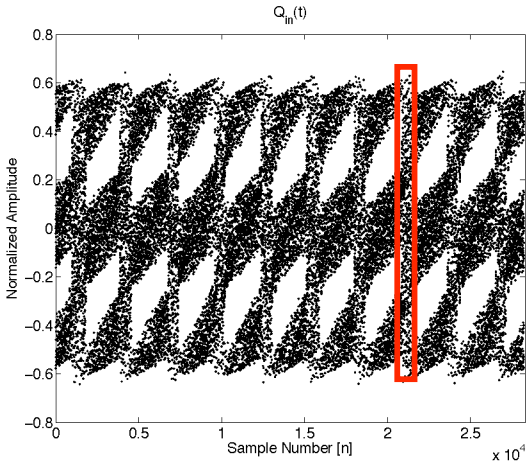

Figure 12 A time domain depiction of a 1KHz Idle Tone

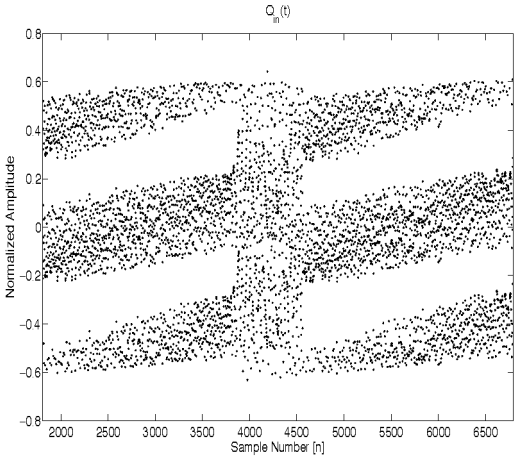

Figure 13 A zoom on a time domain depiction of a 1KHz Idle Tone.

If a zoom is performed on a single time domain region of an idle tone element, as shown in Figure 13, the existence of a vertical stripe can be observed, just like the one previously observed with limit cycles, but with a crucial difference. However, unlike with the limit cycle phenomena described in the previous section, this vertical stripe has a pseudo-random content of data. This means that an idle tone is not formed of a repeatable sequence of data. As depicted in Figure 13, the square region in the middle of one period corresponding to the idle tone has a random pattern and not a striped pattern like limit cycles do. Also notice the existence of various geometrical patterns in the time domain depiction of the idle tone, such as vertical stripes and holes of random data.

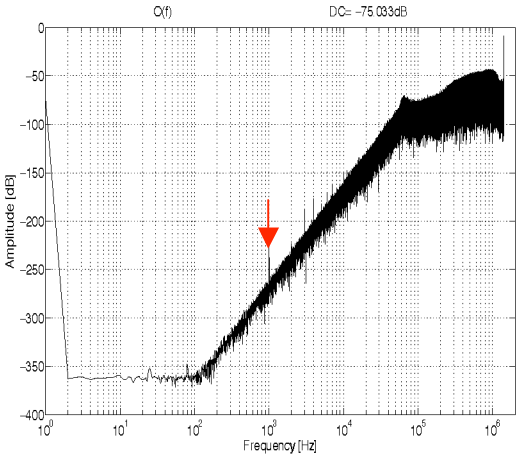

Figure 14 The spectrum of a 1KHz idle tone (1 second FFT, resolution 1Hz).

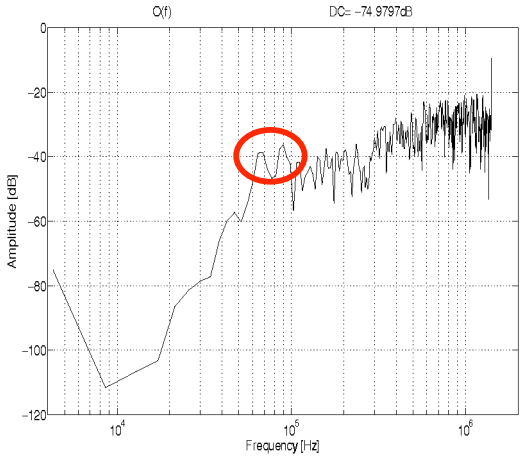

Figure 15 1KHz Idle Spectrum (samples 3886 to 4544)

In Figure 14 the spectrum of one-second of output data of the SDM is presented. The number of complete vertical stripes of random data occurring per second in Figure 12 is directly related to the frequency of the "fundamental" idle tone to appear in the output spectrum of the SDM. There are exactly 1000 vertical stripes and the fundamental idle tone has a frequency of 1000Hz. This fundamental idle tone tends to be, but not necessarily, the idle tone with higher absolute amplitude compared to the noise shaped noise floor. Here, the "fundamental" idle tone does not mean that there are no hidden or visible sub harmonics, but rather that it has happened to be a predictable and traceable idle tone regardless of the SDM transfer function design. In order to comply with standard spectrum analysis terminology, the frequency of the fundamental idle tone (F_{FIT}) will also be referred as the idle tone first harmonic.

If an FFT is perform over a single idle tone, Figure 15, it can be seen that it already contains most of the noise shaped characteristics presented in the one second output spectrum, Figure 14. Even the knee point around 70KHz is present. Idle tones partials are not seen in Figure 15 due to the small amount of data plotted.

In order to generalize this relationship between the time domain input to the quantizer and the frequency domain identification of idle tones, a series of experiments with several SDM designs was performed. The design based on the 5th order SDM previously used in Figure 12 will be used as a comparison reference.

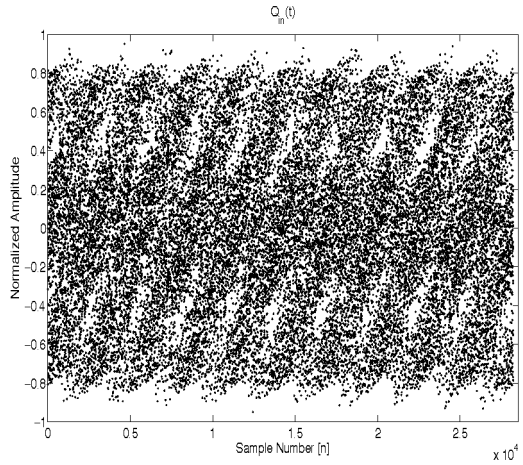

Figure 16 Time domain depiction of the quantiser input for an idle tone. A 5th order SDM, generated from the Toolbox with all zeros at DC, was used.

Schreier's 5th order SDM with initial conditions equal to zero and a DC input of 0.000354308390023V with all zeros at DC was used to generate Figure 16. Although this SDM design is very different from the one investigated in Figure 12-13, the resultant conditions are very similar. The time domain pattern is more blurred, but the number of idle patterns per second continues to be in correspondence with the appearance of a 1KHz fundamental idle tone, as shown in Figure16.

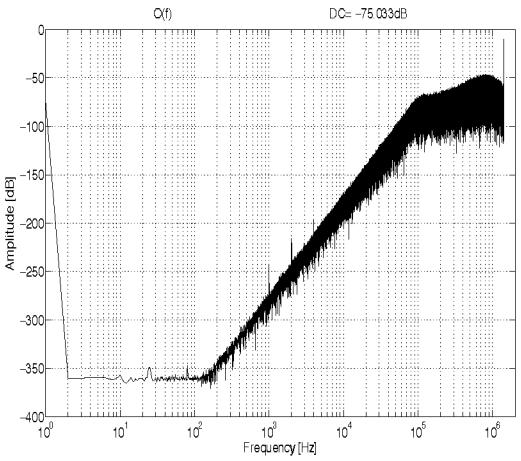

Figure 17 Spectrum of the output bitstream for the same SDM as in Figure 16.

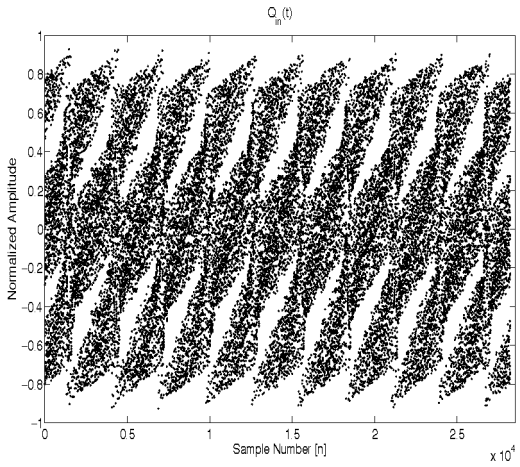

Figure 18 Time domain input to the quantiser for a 3rd order SDM with all zeros at DC.

Comparing Figure 14 and Figure 17, a change in amplitude of the idle partials may be observed between the two SDM designs. Since changing the design did not affect the location of the fundamental idle tone frequency, it appears that although each SDM design may enhance or attenuate idle tone partials they still are related to the fundamental idle tone.

With the aim of observing the influence of SDM order in idle tones, a 3rd order SDM, based on Schreier's Toolbox, was implemented with initial conditions set to zero and a DC input of 0.000354308390023V, where all zeros were at DC. It can be seen in Figure 18 that the 3rd order has a more well-defined idle tone pattern at the input to the quantizer than in Figure 16. It can also be observed in Figure 19 that the lower the order of the SDM, the more idle tones are evident in the output of the SDM. This suggests that smearing of idle tone patterns, in the time domain, improves idle tone behavior. In fact, for a 1st order SDM, under the same conditions, its input to the quantizer will only consist of un-smeared well defined isolated idle tone patterns.

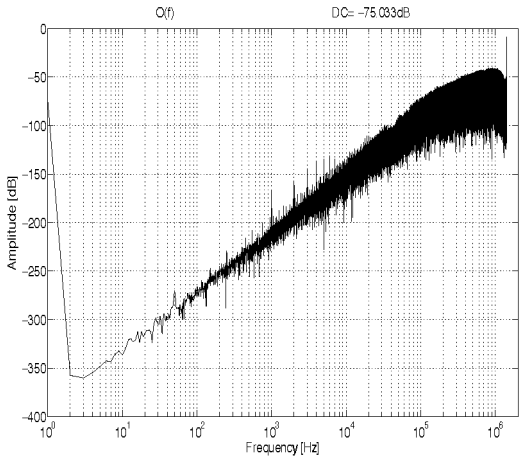

Figure 19 Spectrum of the output bitstream for a 3rd order SDM with all zeros at DC.

To implement a 3rd order SDM with atleast one zero not at DC, Schreier's SDM Toolbox was used with optimization type 1, initial conditions set to zero and a DC input of 0.000354308390023V. A neglectable difference was observed between the 3rd order SDM with all zeros at DC, Figure 18, and the time domain behavior of this SDM. The fundamental idle tone pattern count at the input to the quantizer also remained at the same 1000 idle tone patterns per second.

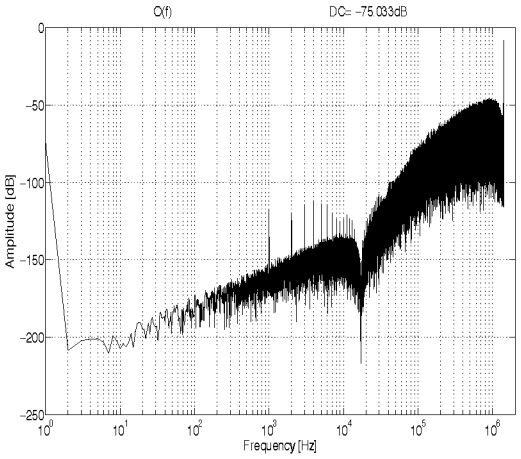

Figure 20 Spectrum of the output bitstream for a 3rd order SDM with atleast one zero not at DC.

However, it can bee seen on Figure 20 that changing the placement of zeros has a significant impact on the output of the SDM spectrum. It can result in a better noise shaping, which may also render the idle tones idle tones more visible.

These results suggest a few possible conclusions concerning the relationship between idle tones and SDM design. It appears that the higher the order of the SDM, the more smeared the idle tone pattern in the time domain. However, changing the SDM zeros has little effect on the idle tones pattern in the time domain. It was also concluded that the idle tone pattern count remains constant regardless of the SDM designs.

4.1. Idle tone DC proportionality

It has been stated that the there is a distinctive idle tone pattern that can be found at the input to the quantizer and that the number of complete occurrences per second gives us the fundamental idle tone frequency. The relationship between the DC input magnitude and the frequency of idle tones may now be explained. By progressively increasing the DC input magnitude (A_{dc}), with values smaller than 0.5V, while tracking the fundamental frequency an important conclusion can be derived; the DC input is proportional to the frequency of the fundamental idle tone (F_{FIT}). This means that as the input signal magnitude is increased, the idle tone frequency will move proportionally towards the Nyquist frequency. Furthermore, if the same DC input is used in a SDM with twice the sampling frequency, the fundamental idle tone frequency is doubled. This means the fundamental idle tone frequency is proportional to the sampling frequency. Simulations verified the following relationship over most of the input magnitude range;

$$F_{FIT}=A_{DC}f_s \qquad (1.)$$

A plot showing the DC magnitude against the fundamental idle tone frequency is presented in Figure 21. Figure 21 was plotted using the 5th order SDM design with an 80Hz corner frequency, with initial conditions set to zero. It depicts a straight line, as expected, except for the very low frequencies and values above 0.5VDC. Any DC amplitude bigger than 0.5V will generate a fundamental idle tone frequency beyond the Nyquist frequency and therefore aliasing behavior should be expected, and will be explained in the next subsection.

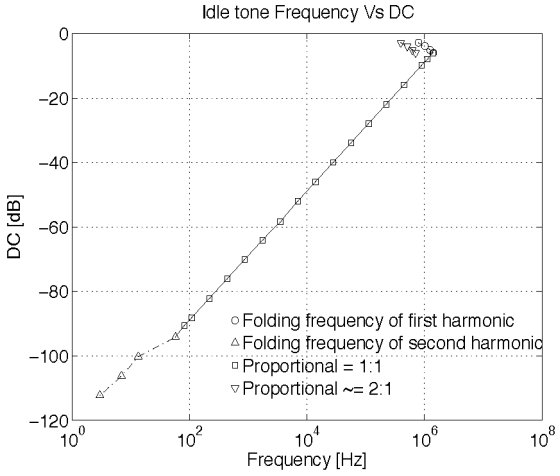

Figure 21 Logarithmic proportionality plot of DC vs. idle tones

The disagreement with Eq. 1 for very low DC inputs remains unexplained. The cause of the disagreement with Eq. (1) may be due to the difficulties in resolution of the FFT due to finite data and to finite precision in low amplitude inputs. For low SDM orders, Eq. (1) extends over a larger range and holds for lower DC inputs (lower idle tone frequencies). This lower end non-linearity remains a subject of further study.

4.2. Idle Tone Aliasing

In order to understand fundamental idle tone aliasing, a folding frequency of the first harmonic (F_{AFIT}) will be plotted. The plot in Figure 22 uses the same 5th order

SDM design with a 80Hz corner frequency, with initial conditions set to zero and a DC input of 0.634534534V. The DC input value is a random number choose by the authors with the only restriction that is should be bigger than 0.5 and within the stability limits of the SDM. Equation (1) can be used to find the fundamental idle tone frequency corresponding to a DC input of 0.634534534V for a Nyquist rate f_h of 44100Hz and an *OSR* of 64. For this particular example the fundamental idle tone frequency is equal to F_{FIT} =1.79091x10^{6}Hz. Because this is greater than half the sampling frequency, 1.41120x10^{6}Hz, it becomes impossible for the SDM to accurately represent such a frequency and therefore it aliases. The equation for calculating the folding frequency value corresponding to the aliased fundamental idle tone is given by,

$$F_{AFIT}=|(Fs-F_{FIT})| \qquad (2.)$$

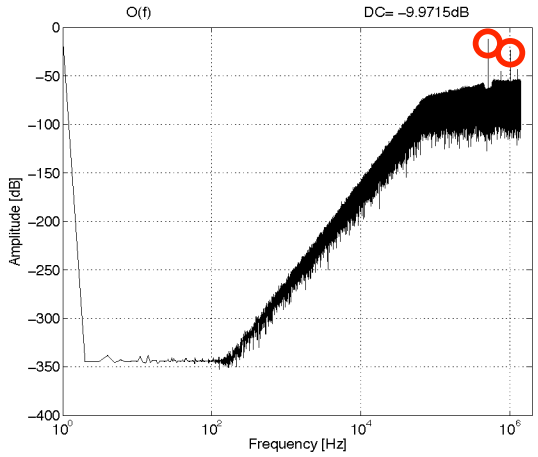

Figure 22 Fundamental idle tone aliasing

Using equation (2) it can be calculated that the folding frequency corresponding to the first harmonic is equal to F_{AFIT} =1.031489x10^{6}Hz. The aliased fundamental idle tone has harmonics that will also alias. In addition, the folding frequency itself has subharmonics. By simply dividing the result of equation (2) by half, the next folding subharmonic, with a value of F_{AFIT}/2= 5.15744x10^{6}Hz, can be calculated. In the same manner, by dividing F_{AFIT} by n, the n^{th} harmonic can be derived. The number of harmonics that alias and the way they interact are dependent on the SDM design. Smaller amplitude partials, which are harder to characterize are usually present, and will be explained in section 4.3.

An important observation, which concerns aliasing, is the upper right idle tone in Figure 14. This type of idle tone is due to rapid alternating bit changes. These changes are averaged and reflected in the spectrum in the form of an idle tone. This idle tone is very close to the Nyquist frequency. The idle tone is commonly present in most SDM designs. This idle tone usually stays close to the Nyquist point for low-level DC values, but whenever there is aliasing present, this idle tone begins to shift to the left. In all cases studied, the idle tone becomes the immediate subharmonic of the folding frequency, which is not the same as the folding idle tone corresponding to the second harmonic of the fundamental idle tone. When aliasing is present the idle tone seems to inter-modulate with other idle tones. Some observations on this are presented in the next subsection.

The implications of idle tone aliasing are quite important because it means that an idle tone located outside the audible range can become audible when having an appropriate amount of DC offset.

4.3. Idle Tone Aliasing and inter-modulation

This concept of inter-modulation of idle tones seems to be supported by the idea that, in many cases all significant idle tones may be related to the fundamental idle tone. To demonstrate this, Figure 23 redepicts Figure 7 in a linear scale with the noticeable idle tones clearly labeled.

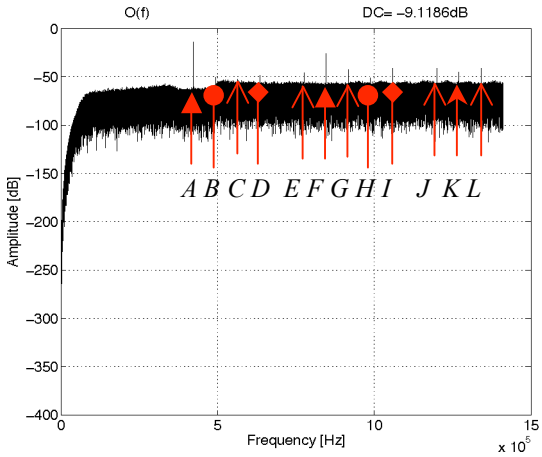

Figure 23 Aliasing and modulation of idle tones, from Figure7 with a linear frequency axis, 0.7A_{DC}.

By using equations (1) and (2) we can obtain the folding idle tone (F) corresponding to the aliased fundamental idle tone.

From (1) F_{FIT}=1.97568 x10^6Hz
From (2) F= F_{AFIT} =8.46720x10^5Hz
By using F_{FIT} and F_{AFIT} we can derive the inter-modulated partials:
A=F/2=4.23360x10^5Hz
H= F_{FIT}/2=9.87840 x10^5Hz
B= F_{FIT} /4=4.93920 x10^5Hz
K=A+F=1.27008x10^6Hz
D=F-(F/4)= 6.35040x10^5Hz
I= F+(F/4)= 1.05840x10^6Hz
J=(A+F)-(B-A)=1.19952 x10^6Hz
L=(A+F)+(B-A)= 1.34064x10^6Hz
C=(B-A)+ B= 5.64480x10^5Hz
E=F-(B-A)= 7.76160x10^5Hz
G=F+(B-A)=9.17280 x10^5Hz

This same procedure can be used to find the two smaller amplitude partials present in Figure 22. For simplicity we will name this small amplitude partials from left to right O and P.

From (1) F_{FIT}= 1.79091x10^6Hz
From (2) F_{AFIT} =1.03149x10^6Hz
O=(2x F_{FIT})–(f_s)=7.59420x10^5Hz
P= [O-(F_{AFIT}/2)]+ F_{AFIT} = 1.27517x10^6Hz

5. IDLE TONE OBSERVATIONS

DC idle tones are a phenomenon, which for a bounded region, have at least one partial at a frequency which is proportionally related to the DC input. The idle tone frequencies occurring in the spectral output of the SDM can be directly related to the number of idle pattern occurrences in the time domain input to the quantizer. When the spectral output of the SDM corresponding to a single idle tone pattern is plotted, it cannot be isolated from the noise shaped noise. These observations imply that idle tones are the result of a quasi-repeatable string of data as suggested by [1].

Idle tones are susceptible to aliasing. This research has found that other idle partials are related to this fundamental idle tone. The results also suggest that fundamental idle tone frequency is independent of the order and design of the SDM.

6. CONCLUSIONS AND FURTHER STUDY

The difference between the idle tone phenomenon and limit cycle has been stated. Limit cycle phenomena have been classified into limit cycles, short limit cycles and periodic short limit cycles. The relationship between each of these phenomena and the spectral output has also been investigated.

The concept of fundamental idle tones, alias idle tones and idle tones due to rapid alternating bit changes has been stated. For idle tones, a relationship between the time domain input to the quantizer and the spectral output of the SDM has been shown. A corresponding input to the quantizer pattern that identifies an idle tone has been shown. A bounded proportionality between the DC input and the frequency of the idle tone has been found. Behavior regarding idle tone aliasing has been introduced. Idle tone inter-modulation has been verified.

However

Idle tone modulation activity has been reported by [5] and has been confirmed by this research, but full understanding of its behavior remain unexplained. Fundamental idle tone sub-harmonics, and idle sub-partials, in general remain to be explained. Furthermore, the full details of the interaction between idle tones and limit cycles are still not understood.

7. APPENDIX A: SIMULATION COEFFICIENTS

The coefficients presented next determine the transfer function of the SDMs used for this paper. Nomenclature of the coefficients for the first SDM is in accordance to the pseudo-code presented at the end of the paper in [3]. Nomenclature for the SDM used with the Schreier's toolbox is in accordance with the function <SimulaterDSM>. If SDM optimization is to be performed, the function <synthesizeNTF> can be used to obtain the coefficients. More information on these functions can be found in [13]. The toolbox can be downloaded from [7]. When redoing the simulations it is important to make sure that all initial conditions are set to zero, OSR=64 and H_f=44100Hz

The coefficients used for the 5th order, 80Hz corner frequency SDM based on Reefman et al. [3] are:
$c0$= 0.5761069262, $c1$= 0.1624753515,
$c2$= 0.0276093301, $c3$= 0.0028053934,
$c4$= 0.0001360361,

f0,f1=0
s0,s1,s2,s3,s4=0
Note: The first input sample was forced to be zero $X_{in0}=0$

Schreier's SDM Toolbox [7], 5th order SDM with no optimization. (optimization=0)
a0= 0.0006554819, *a1*= 0.0088674279,
a2= 0.0555460310, *a3*= 0.2521301586,
a4= 0.5555555560,
g0= 0.0000000000, *g1*= 0.0000000000,
b0= 0.0006554819, *b1*= 0.0088674279,
b2= 0.0555460310, *b3*= 0.2521301586,
b4= 0.5555555560, *b5*= 1.0000000000,
c0, c1, c2,c3,c4= 1.0000000000

Schreier's SDM Toolbox, 3th order SDM with no optimization (optimization=0)
a0= 0.0439826180, *a1*= 0.2441530790,
a2= 0.5555857817,
g0= 0.0000000000,
b0= 0.0439826180, *b1*= 0.2441530790,
b2= 0.5555857817, *b3*= 1.0000000000,
c0, c1, c2= 1.0000000000

Schreier's SDM Toolbox, 3th order SDM optimized (optimization=1)
a0= 0.0440836028, *a1*= 0.2430790784,
a2= 0.5559071001,
g0= 0.0014455687,
b0= 0.0440836028, *b1*= 0.2430790784,
b2= 0.5559071001, *b3*= 1.0000000000,
c0, c1, c2= 1.0000000000

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